Accurate Statistical-Based DDR4 Margin Estimation using SSN Induced Jitter Model

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**DDR4 Highlights**

- **Highlights:**
  - Lower VDD voltage and Pseudo-Open Drain (POD) reduced power consumption by 40%
  - Internal VREF training performed within the IC receiver to optimize VREF level. Retraining at regular intervals
  - Data lines are calibrated at the IC to reduce their skew to the strobe
  - Data bus inversion (DBI)

<table>
<thead>
<tr>
<th>Specification</th>
<th>DDR2</th>
<th>DDR3</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>1.8 V</td>
<td>1.5 / 1.35 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Per Pin Data Rate (Mbps)</td>
<td>400-1066</td>
<td>800-2133</td>
<td>1600-3200</td>
</tr>
<tr>
<td>Channel Bandwidth (GBps)</td>
<td>3.2-8.5</td>
<td>6.4-17</td>
<td>12.8-25.6</td>
</tr>
<tr>
<td>Component Density</td>
<td>512 MB–2 GB</td>
<td>1-8 GB</td>
<td>2-16 GB</td>
</tr>
</tbody>
</table>
Timing Margin vs. BER

- Requires new specs beyond traditional timing margin:
  - Higher data rate – reduced UI and smaller margin
  - Reduced VDDQ to achieve power consumption spec
  - Timing margin is eroded by ISI and RJ
  - Adding a safety margin creates over-engineered solutions

![Shrinking Timing Margins in Picoseconds](Image Source: Altera)
New JEDEC DQ Specification

- Receiver requirements defined by masks instead of setup / hold and DC voltage swings

- Bit Error Rate (BER) Specification:
  - Simpler definition of DRAM requirements and system design
  - Bit Error Rate (BER) spec recovers timing and noise margin
  - Eliminates troublesome slew rate derating
  - Jitter includes the sum of deterministic and random jitter terms for a specified BER
  - The design specification is BER < $1 \times 10^{-16}$

- How many bits for $1 \times 10^{-16}$ BER?
  - 10 quadrillion bits ($1/10^{-16}$), equivalent to 125,000 Peta Bytes
Bit-by-bit (SPICE-Like) vs. Statistical Approach

- **Bit-by-bit (SPICE-Like, Transient) Approach**
  - Bit-by-bit simulation takes too long to run for 10 quadrillion bits
  - At least, 1 million bits ($1e^6$) is required to do jitter separation and predict eye opening accurately using Dual-Dirac extrapolation with Bit-by-bit approach
  - Example: 4587 seconds for a simple DQ test case

- **Statistical Approach (13 seconds, 350X faster)**
  - Statistical calculation for DQ and DQs eye probabilities at ultra low BER in seconds not days without running an actual bit sequence
  - No need for risky dual-Dirac extrapolation
  - Example: 13 seconds for the simple DQ test case
Simultaneous Switching Noise (SSN)

- SSN noise is generated when all drivers switch concurrently with fast rising/falling edge

- Two primary SSN mechanisms are:
  - Crosstalk
    - Mutual coupling from aggressor signals to victim
  - Delta-I noise due to the inductance of both power and ground plane
    - The switching current on both power and ground planes induces a fluctuating voltage drop, by $L \cdot \frac{di}{dt}$.
    - The voltage drop is proportional to the inductance and switching speed
Delta-I Noise With Statistical Approach

- **Assumptions made in statistical approach**
  - Statistical methodology assumes the system to be LTI (Linear Time Invariant)
  - The amplitude and jitter noise by crosstalk and ISI are well taken care of by the statistical approach

- **Dilemma:**
  - Delta-I induced amplitude and jitter noise are time variant, so they are not taken into consideration with the statistical approach
  - For the ultra-low BER value, $1e^{-16}$, the statistical approach is required

1. Transient analysis to get an impulse response of channel, TX, and RX
2. Statistical analysis with the statistical distribution of a conceptually infinite non-repeating bit pattern
Solution - Mask Correction Factor (MCF)

- **Definition of MCF:**
  - The difference of eye height and eye width, one with and the other without delta-I noise contribution
    - Eye height difference – Amplitude noise correction factor
    - Eye width difference – Jitter noise correction factor

- **Usage of MCF:**
  - Apply to the mask data to compensate delta-I induced noise for the statistical analysis
  - Correct the eye height and eye width value at a certain BER level

<table>
<thead>
<tr>
<th>Example:</th>
<th>Amplitude MCF</th>
<th>Jitter MCF</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>25 mV</td>
<td>19 ps</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th></th>
<th>DDR4 DQ Mask in JEDEC Spec</th>
<th>New DQ Mask After Correction factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Width</td>
<td>0.2 UI</td>
<td>0.24 UI</td>
</tr>
<tr>
<td>Eye Height</td>
<td>130 mv</td>
<td>155 mv</td>
</tr>
</tbody>
</table>
MCF Extraction Procedure

- **Steps to extract MCF:**
  - Run Transient simulations on two cases, one with PDN and the other without PDN.
  - Find the eye height and eye width values at the expected BER level respectively.
  - Extract the mask correction factor by subtracting the values of these two cases for the amplitude and jitter MCF.

- **Note for PDN model:**
  - Higher frequency model to avoid any extrapolation errors and accurately model the switching speed.

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<th>Jitter MCF</th>
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Total current draw vs. number of DQ lines

- If the bit pattern on each of 64 DQ lines is identical, the total current draw from the source will increase linearly proportional to the number of DQ lines included. But in real case, the bit pattern is random, so it doesn’t have the linear relationship.
- Extract MCF with all 64 DQ line running by the non-identical bit patterns.

Cases with 4, 8, 12, 16, 20, 24, 28, 32, 36, 48, and 64 DQs DQ lines
Test Example for MCF vs. # of DQ Lines

- **Transmitter**
  - 64 PRBS with a different seed value
  - 64 “kintexu.ibs” Power-Aware IBIS models

- **Results**
  - Amplitude correction factor:
    - 49 mV with 64 DQs and 24 mV with 16 DQs
  - Jitter correction factor:
    - 25 ps with 64 DQs and 6 ps with 16 DQs

- **Receiver**
  - 64 Micron “z80a_v5p0.ibis model”
  - Package models included

![Graphs showing comparison between W/O PDN and With PDN 16 Lines, With PDN 64 Lines](image-url)
Xilinx® KCU 105 FPGA Platform Board

- Provides a hardware environment for developing and evaluation designs targeting the Ultrascale™ XCKU040-2FFVA1156E device
- Provides features common to many evaluation systems including DDR4, HDMI, SFP+, PCIe, Ethernet PHY, etc
- 9.27 x 5 inch, 16 layers PCB

DDR4 Memory

- 2GB Micron 4 DDR4 component memory (four [256 Mb x 16] devices)
- 64 DQ lines between FPGA and DDR4 memory with a single Power Deliver Network
MCF Extraction for KCU105 Board

- **MCF Extraction**
  - Pre-layout models used for the channel
  - Transient Simulation w/ and w/o PDN on DQ lines with $10^6$ bits
  - Significant increase of noise to amplitude and jitter
    - Amplitude, jitter correction factor: 94 mV, 16 ps

### Table

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/O PDN</td>
<td>3.917E-10, 0.301</td>
</tr>
<tr>
<td>W/ PDN</td>
<td>3.750E-10, 0.287</td>
</tr>
</tbody>
</table>

### Diagram

- TX
- RX
- CH
- CH
- CH
- **PCB EM Modeling**
  - Accurate EM models for PCB, which include channels (DQ, DQs, etc) and PDN
  - Include only one I/O Bank (16 bits) for a faster EM model generation assuming minimal crosstalk between I/O banks
  - Vendor supplied de-coupling capacitor models

- **DDR Bus Simulation (Statistical Approach)**
  - Simulations at two BER level, $1\times 10^{-8}$ and $1\times 10^{-16}$

- @ BER = $1\times 10^{-8}$
  - Eye height = 347 mV, Eye width = 356 ps

- @ BER = $1\times 10^{-16}$
  - Eye height = 374 mV, Eye width = 348 ps
Measurement Setup

- **Measurement:**
  - Keysight’s DSAV334A Infinium Oscilloscope
  - N6462A DDR4 Compliance Test Application
  - Measured on DQ35 at 2400 Mbps speed grade with 109 million bits, which is close to $1 \times 10^{-8}$ BER
**Measured Data**

- **Measurement at 109 million bits:**
  - Eye Width – 339 ps
  - Eye Height – 271 mV

<table>
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<th>Measurement Result (@1E^-8 BER)</th>
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<tr>
<td>Eye Width</td>
<td>339 ps</td>
</tr>
<tr>
<td>Eye Height</td>
<td>271 mV</td>
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</table>
Side-By-Side Comparison

- Statistical analysis vs. measured comparison on DQ35 – No correction:
  - Reasonable agreement
  - Larger amplitude and jitter noise with the measured data due to the delta-I noise contribution
Corrected Mask – Still Within Spec!

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<tr>
<td>WidthAtBER</td>
<td>3.229E-10</td>
</tr>
<tr>
<td>HeightAtBER</td>
<td>0.360</td>
</tr>
<tr>
<td>TimingMarginUL</td>
<td>6.771E-11</td>
</tr>
<tr>
<td>TimingMarginUR</td>
<td>6.354E-11</td>
</tr>
<tr>
<td>TimingMarginLL</td>
<td>6.354E-11</td>
</tr>
<tr>
<td>TimingMarginLR</td>
<td>6.354E-11</td>
</tr>
<tr>
<td>VoltageMarginUL</td>
<td>0.028</td>
</tr>
<tr>
<td>VoltageMarginUR</td>
<td>0.065</td>
</tr>
<tr>
<td>VoltageMarginLL</td>
<td>0.034</td>
</tr>
<tr>
<td>VoltageMarginLR</td>
<td>0.071</td>
</tr>
<tr>
<td>MinVoltageMarginU</td>
<td>0.028</td>
</tr>
<tr>
<td>MinVoltageMarginL</td>
<td>0.034</td>
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| | Amplitude MCF | Jitter MCF |
|-----------------|--------------|
| DDR4 DQ Mask in JEDEC Spec | New DQ Mask After Correction factor |
| Eye Width        | 0.2 UI       | 0.23 UI     |
| Eye Height       | 130 mV       | 224 mV      |

<table>
<thead>
<tr>
<th></th>
<th>time, psec</th>
</tr>
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<tbody>
<tr>
<td>Eye Width</td>
<td>0.2 UI</td>
</tr>
<tr>
<td>Eye Height</td>
<td>130 mV</td>
</tr>
</tbody>
</table>
**Eye Height and Width with MCF Applied**

- **Excellent agreement**:
  - 2% eye width difference on simulation vs. measured @ 1e-8 BER
  - 2.2% eye height difference on simulation vs. measured @ 1e-8 BER

<table>
<thead>
<tr>
<th></th>
<th>DDR BUS Sim Result @ 1E-16 BER</th>
<th>DDR BUS Sim Result @ 1E-8 BER</th>
<th>Measurement Result (@1E-8 BER)</th>
<th>Sim/Measure Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>W/O correction factor</td>
<td>With correction factor</td>
<td>W/O correction factor</td>
<td>With correction factor</td>
</tr>
<tr>
<td>Eye Width</td>
<td>323 ps</td>
<td>307 ps</td>
<td>348 ps</td>
<td>332 ps</td>
</tr>
<tr>
<td>Eye Height</td>
<td>360 mv</td>
<td>266 mv</td>
<td>371 mv</td>
<td>277 mv</td>
</tr>
</tbody>
</table>

*Compared*
Conclusion

- Statistical simulation approach must be used for DDR4 to get an ultra-low BER, $10^{-16}$.
- Statistical simulation approach assumes the system to be linear, so the delta-I noise contribution for SSN is ignored.
- Proposed solution using the mask correction factor (MCF) improves the accuracy of DDR4 statistical simulation by compensating the delta-I noise contribution.
- Simulated results with MCF agree well to the measured data.
References


Thank you!

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QUESTIONS?