Accurate Statistical-Based DDR4 Margin Estimation using SSN Induced Jitter Model

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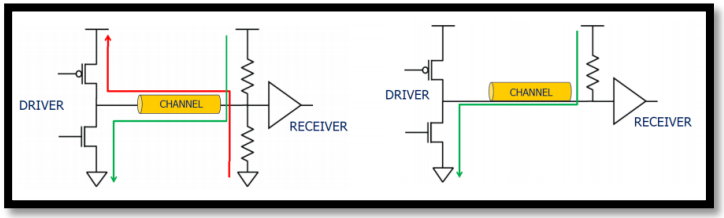
DDR4 Highlights

- **Highlights:**
  - Lower VDD voltage and Pseudo-Open Drain (POD) reduced power consumption by 40%
  - Internal VREF training performed within the IC receiver to optimize VREF level. Retraining at regular intervals
  - Data lines are calibrated at the IC to reduce their skew to the strobe
  - Data bus inversion (DBI)

Specification	DDR2	DDR3	DDR4
Voltage	1.8 V	1.5 / 1.35 V	1.2 V
Per Pin Data Rate (Mbps)	400-1066	800-2133	1600-3200
Channel Bandwidth (GBps)	3.2-8.5	6.4-17	12.8-25.6
Component Density	512 MB–2 GB	1-8 GB	2-16 GB

Image Source: Micron Technology

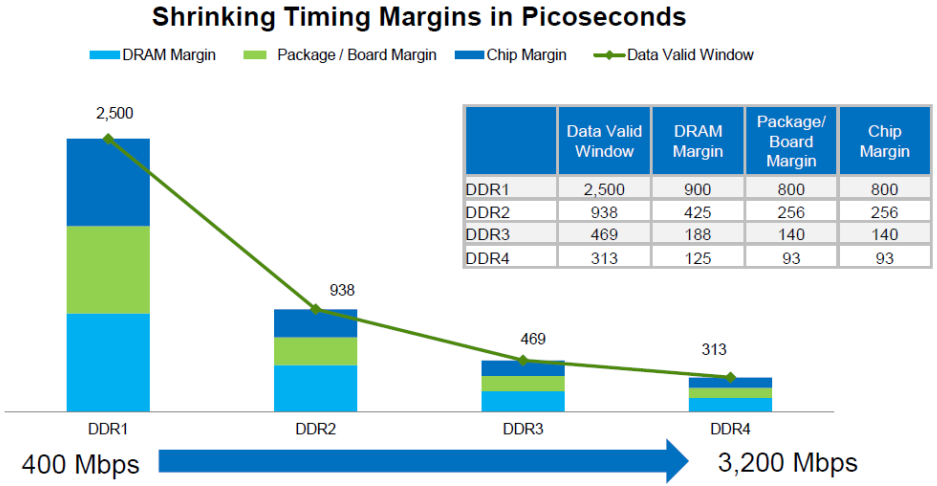


DDR3 Push-Pull

DDR4 Pseudo-Open Drain

Timing Margin vs. BER

- **Requires new specs beyond traditional timing margin:**
  - Higher data rate – reduced UI and smaller margin
  - Reduced VDDQ to achieve power consumption spec
  - Timing margin is eroded by ISI and RJ
  - Adding a safety margin creates over-engineered solutions



	Data Valid Window	DRAM Margin	Package/ Board Margin	Chip Margin
DDR1	2,500	900	800	800
DDR2	938	425	256	256
DDR3	469	188	140	140
DDR4	313	125	93	93

Image Source: Altera

New JEDEC DQ Specification

- **Receiver requirements defined by masks instead of setup / hold and DC voltage swings**
- **Bit Error Rate (BER) Specification:**
  - Simpler definition of DRAM requirements and system design
  - Bit Error Rate (BER) spec recovers timing and noise margin
  - Eliminates troublesome slew rate derating
  - Jitter includes the sum of deterministic and random jitter terms for a specified BER
  - The design specification is BER < $1e^{-16}$
- **How many bits for $1e^{-16}$ BER?**
  - 10 quadrillion bits (1/ $1e^{-16}$), equivalent to 125,000 Peta Bytes

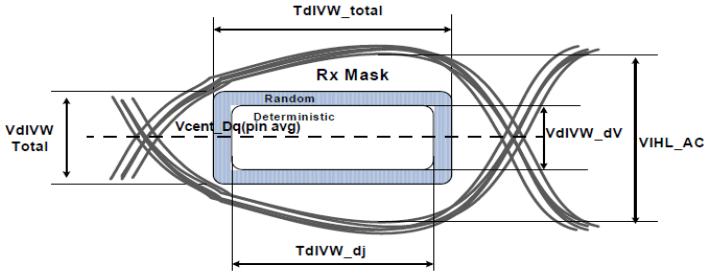


Table 103 — DRAM DQs In Receive Mode; * UI=tck(avg)min/2

Symbol	Parameter	1600,1866,2133		2400		2666,3200		Unit	NOTE
		min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	136 (note12)	-	tbd	-	tbd	mV	1,2,4,6
VdIVW_dV	Rx Mask voltage - deterministic	-	136	-	tbd	-	tbd	mV	1,5,13
TdIVW_total	Rx timing window total	-	0.2 (note12)	-	tbd	-	tbd	UI*	1,2,4,6
TdIVW_dj	Rx deterministic timing	-	0.2	-	tbd	-	tbd	UI*	1,5, 13
VIHL_AC	DQ AC input swing pk-pk	186	-	tbd	-	tbd	-	mV	7
TdIPW	DQ input pulse width	0.58		tbd		tbd		UI*	8
Tdqs_off	DQ to DQS Setup offset	-	tbd	-	tbd	-	tbd	UI*	9
Tdqh_off	DQ to DQS Hold offset	-	tbd	-	tbd	-	tbd	UI*	9
Tdqs_dd_off	DQ to DQ Setup offset	-	tbd	-	tbd	-	tbd	UI*	10
Tdqh_dd_off	DQ to DQ Hold offset	-	tbd	-	tbd	-	tbd	UI*	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	tbd	9	tbd	tbd	tbd	tbd	V/ns	11

NOTE :
1. Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(pin avg). The data Rx mask is applied per bit and should include voltage and temperature drift terms. The design specification is BER <1e-16 and how this varies for lower BER is tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tbd).

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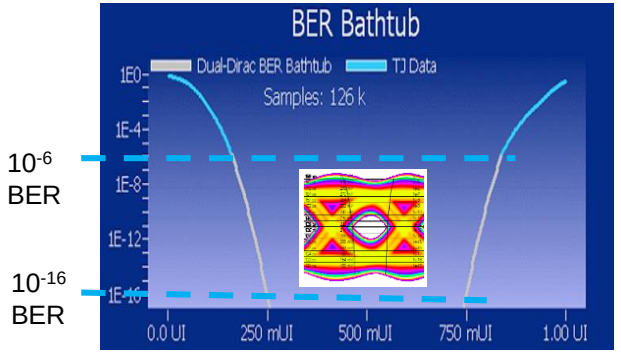
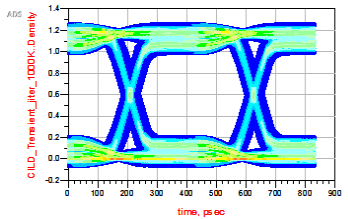
Bit-by-bit (SPICE-Like) vs. Statistical Approach

- **Bit-by-bit (SPICE-Like, Transient) Approach**
  - Bit-by-bit simulation takes too long to run for 10 quadrillion bits
  - At least, 1 million bits ($1e^{-6}$) is required to do jitter separation and predict eye opening accurately using Dual-Dirac extrapolation with Bit-by-bit approach
  - Example: 4587 seconds for a simple DQ test case
- **Statistical Approach (13 seconds, 350X faster)**
  - Statistical calculation for DQ and DQs eye probabilities at ultra low BER in seconds not days without running an actual bit sequence
  - No need for risky dual-Dirac extrapolation
  - Example: 13 seconds for the simple DQ test case

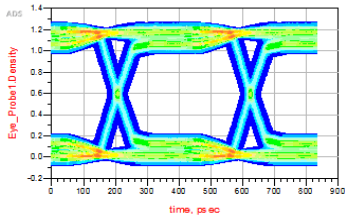


Transient 1M Bits 4587 secs



measurement	...er_1000K..Summary
WidthAtBER	3.158E-10
HeightAtBER	0.826

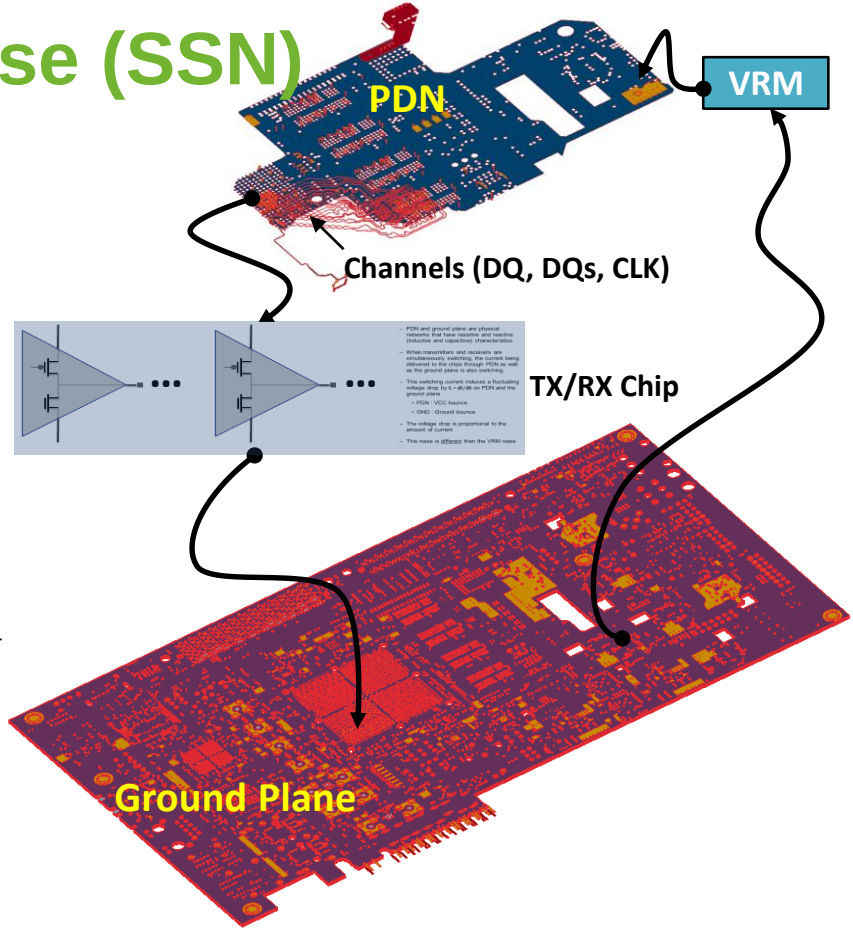
Statical Simulation 13 secs



measurement	...e_Probe1.Summary
WidthAtBER	3.154E-10
HeightAtBER	0.826

Simultaneous Switching Noise (SSN)

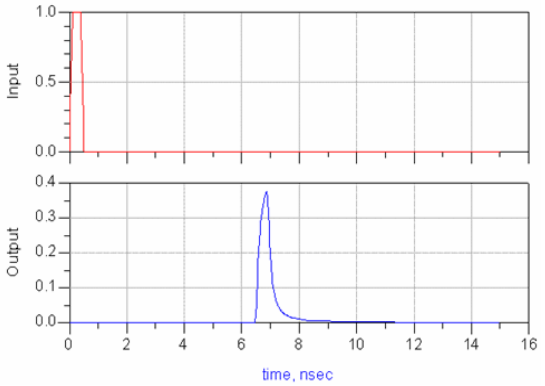
- **SSN noise is generated when all drivers switch concurrently with fast rising/falling edge**
- **Two primary SSN mechanisms are:**
  - Crosstalk
    - Mutual coupling from aggressor signals to victim
  - Delta-I noise due to the inductance of both power and ground plane
    - The switching current on both power and ground planes induces a fluctuating voltage drop, by $\mathbf{L} * \mathbf{di}/\mathbf{dt}$.
    - The voltage drop is proportional to the inductance and switching speed



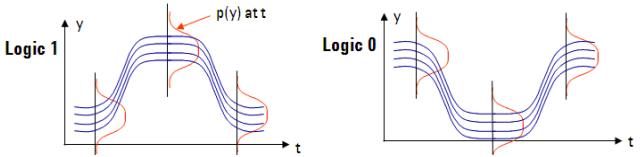
Delta-I Noise With Statistical Approach

- **Assumptions made in statistical approach**
  - Statistical methodology assumes the system to be LTI (Linear Time Invariant)
  - The amplitude and jitter noise by crosstalk and ISI are well taken care of by the statistical approach
- **Dilemma:**
  - Delta-I induced amplitude and jitter noise are time variant, so they are not taken into consideration with the statistical approach
  - For the ultra-low BER value, $1e^{-16}$, the statistical approach is required

1. Transient analysis to get an impulse response of channel, TX, and RX

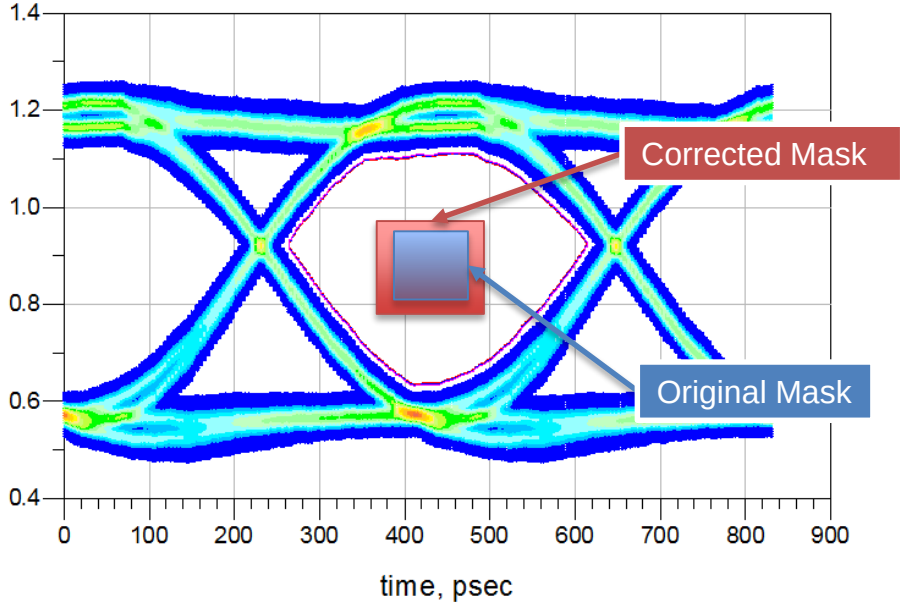


2. Statistical analysis with the statistical distribution of a conceptually infinite non-repeating bit pattern



Solution - Mask Correction Factor (MCF)

- **Definition of MCF:**
  - The difference of eye height and eye width, one with and the other without delta-I noise contribution
    - Eye height difference – Amplitude noise correction factor
    - Eye width difference – Jitter noise correction factor
- **Usage of MCF:**
  - Apply to the mask data to compensate delta-I induced noise for the statistical analysis
  - Correct the eye height and eye width value at a certain BER level



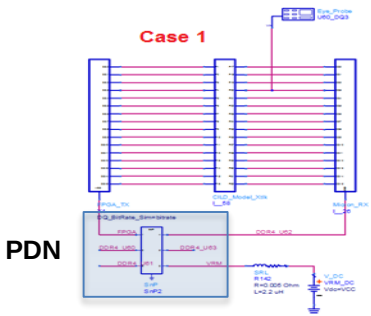
Example:

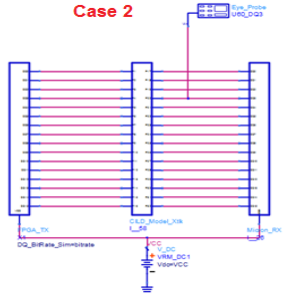
Amplitude MCF	Jitter MCF
25 mV	19 ps

	DDR4 DQ Mask in JEDEC Spec	New DQ Mask After Correction factor
Eye Width	0.2 UI	0.24 UI
Eye Height	130 mv	155 mv

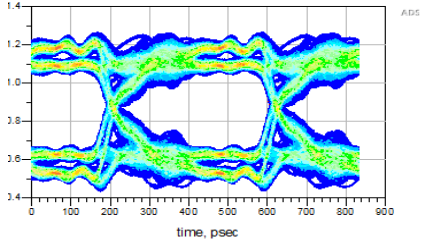
MCF Extraction Procedure

- **Steps to extract MCF:**
  - Run Transient simulations on two cases, one with PDN and the other without PDN.
  - Find the eye height and eye width values at the expected BER level respectively
  - Extract the mask correction factor by subtracting the values of these two cases for the amplitude and jitter MCF
- **Note for PDN model:**
  - Higher frequency model to avoid any extrapolation errors and accurately model the switching speed



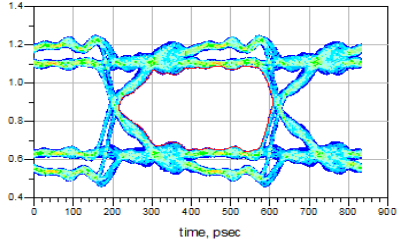


Case 1 With PDN



measurement	...3.Summary
WidthAtBER	3.771E-10
HeightAtBER	0.423

Case2 W/O PDN



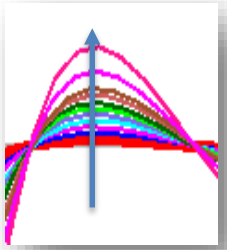
measurement	...B..Summary
WidthAtBER	3.958E-10
HeightAtBER	0.448

Amplitude MCF	Jitter MCF
25 mV	19 ps

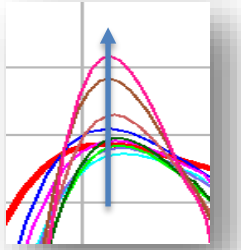
Relationship Between MCF and # of DQ Lines

- **Total current draw vs. number of DQ lines**
  - If the bit pattern on each of 64 DQ lines is identical, the total current draw from the source will increase linearly proportional to the number of DQ lines included. But in real case, the bit pattern is random, so it doesn't have the linear relationship
  - Extract MCF with all 64 DQ line running by the non-identical bit patterns

Cases with 4,8,12,16,20,24,28,32,36,48, and 64 DQs DQ lines

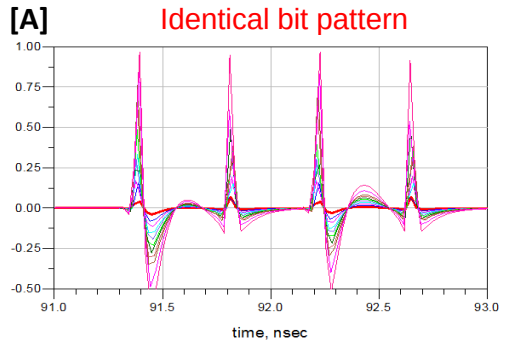


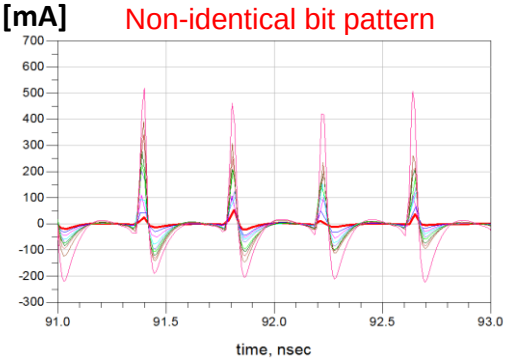
Identical bit pattern



Non-identical bit pattern

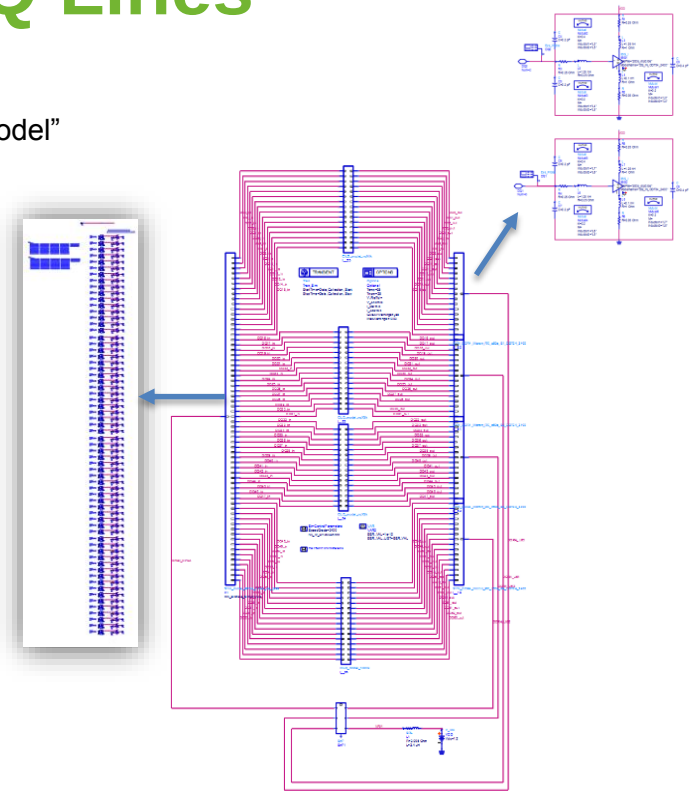
Total Current Draw



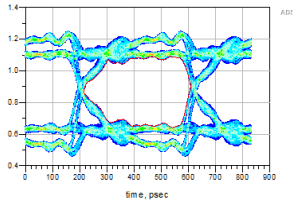


Test Example for MCF vs. # of DQ Lines

- **Transmitter**
  - 64 PRBS with a different seed value
  - 64 “kintexu.ibs” Power-Aware IBIS models
- **Results**
  - Amplitude correction factor:
    - **49 mV with 64 DQs and 24 mV with 16 DQs**
  - Jitter correction factor:
    - **25 ps with 64 DQs and 6 ps with 16 DQs**
- **Receiver**
  - 64 Micron “z80a_v5p0.ibis model”
  - Package models included

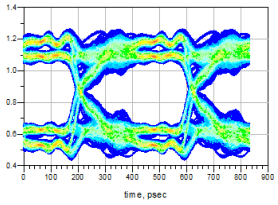


W/O PDN



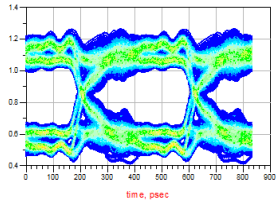
measurement	...B_Summary
WidthAtBER	3.958E-10
HeightAtBER	0.448

With PDN 16 Lines



measurement	...3.Summary
WidthAtBER	3.771E-10
HeightAtBER	0.423

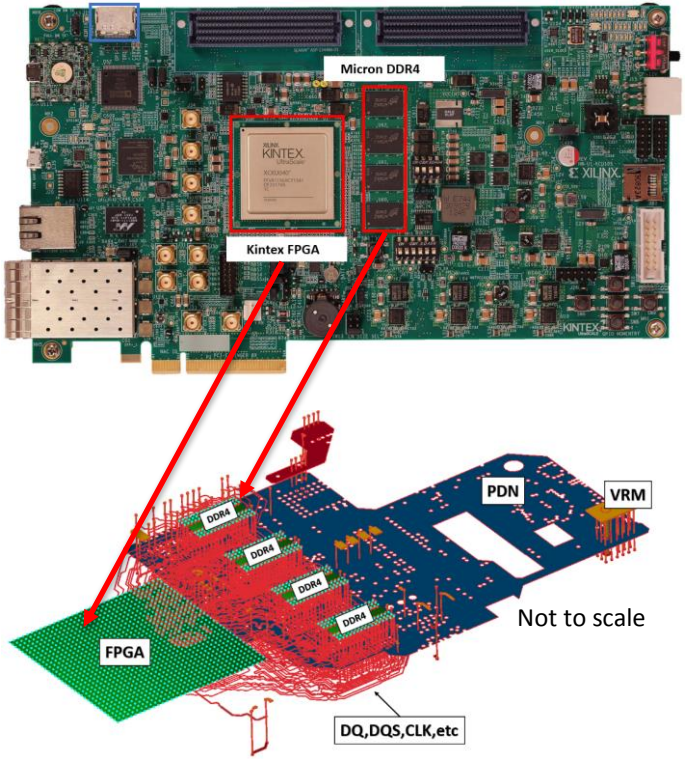
With PDN 64 Lines



measurement	.....Summary
WidthAtBER	3.708E-10
HeightAtBER	0.399

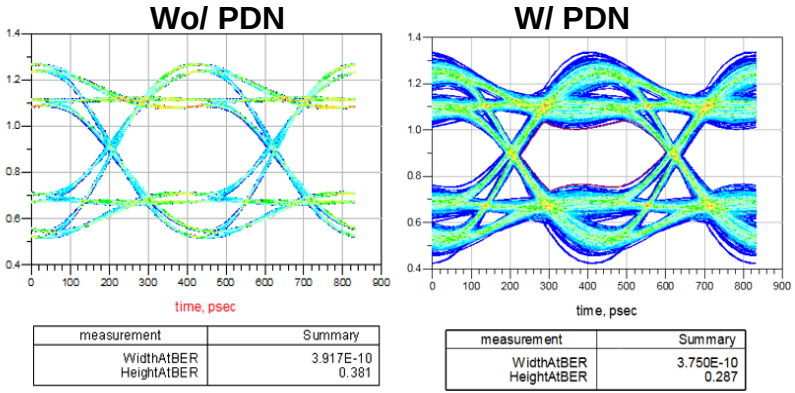
Solution Validation

- **Xilinx® KCU 105 FPGA Platform Board**
  - Provides a hardware environment for developing and evaluation designs targeting the Ultrascale™ XCKU040-2FFVA1156E device
  - Provides features common to many evaluation systems including DDR4, HDMI, SFP+, PCIE, Ethernet PHY, etc
  - 9.27 x 5 inch, 16 layers PCB
- **DDR4 Memory**
  - 2GB Micron 4 DDR4 component memory (four [256 Mb x 16] devices)
  - 64 DQ lines between FPGA and DDR4 memory with a single Power Deliver Network



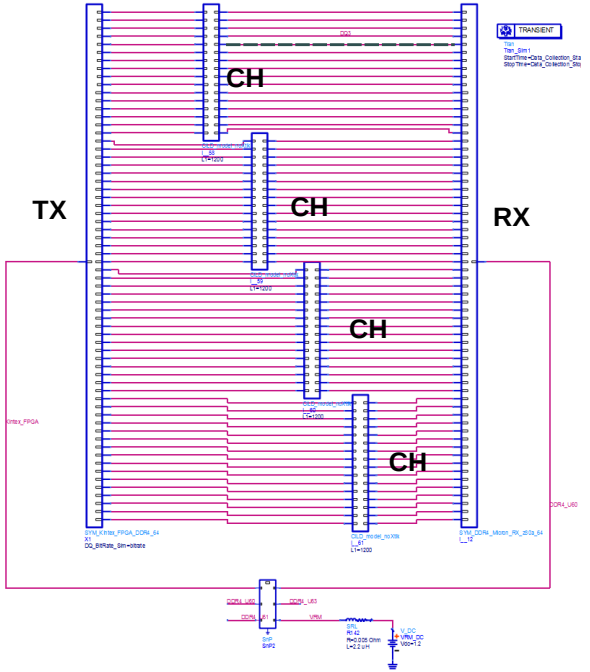
MCF Extraction for KCU105 Board

- **MCF Extraction**
  - Pre-layout models used for the channel
  - Transient Simulation w/ and w/o PDN on DQ lines with $1e^6$ bits
  - Significant increase of noise to amplitude and jitter
    - Amplitude, jitter correction factor: 94 mV, 16 ps



measurement	Summary
WidthAtBER	3.917E-10
HeightAtBER	0.381

measurement	Summary
WidthAtBER	3.750E-10
HeightAtBER	0.287

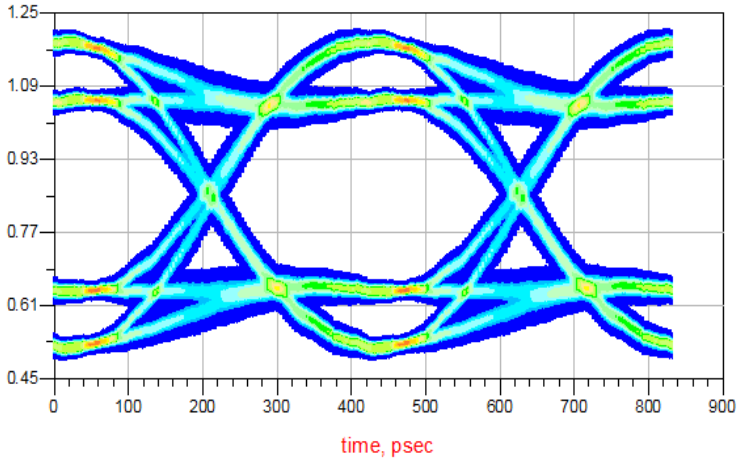


Amplitude MCF	Jitter MCF
94 mV	16 ps

Statistical Analysis – KCU105 Board

- **PCB EM Modeling**
  - Accurate EM models for PCB, which include channels (DQ, DQs, etc) and PDN
  - Include only one I/O Bank (16 bits) for a faster EM model generation assuming minimal crosstalk between I/O banks
  - Vendor supplied de-coupling capacitor models
- **DDR Bus Simulation (Statistical Approach)**
  - Simulations at two BER level, $1e^{-8}$ and $1e^{-16}$
- **@ BER = $1e^{-8}$**
  - Eye height = 347 mV, Eye width = 356 ps
- **@ BER = $1e^{-16}$**
  - Eye height = 374 mV, Eye width = 348 ps

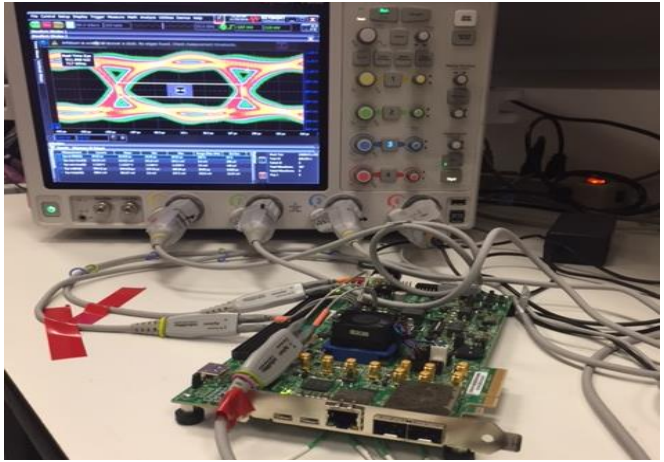
DQ35 Eye Diagram

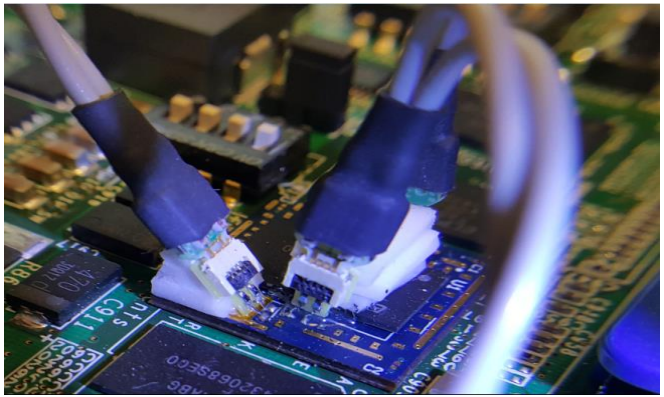


measurement	@ 1E-16 BER	@ 1E-8 BER
WidthAtBER	3.479E-10	3.563E-10
HeightAtBER	0.367	0.374

Measurement Setup

- **Measurement:**
  - Keysight's DSAV334A Infiniium Oscilloscope
  - N6462A DDR4 Compliance Test Application
  - Measured on DQ35 at 2400 Mbps speed grade with 109 million bits, which is close to $1e^{-8}$ BER

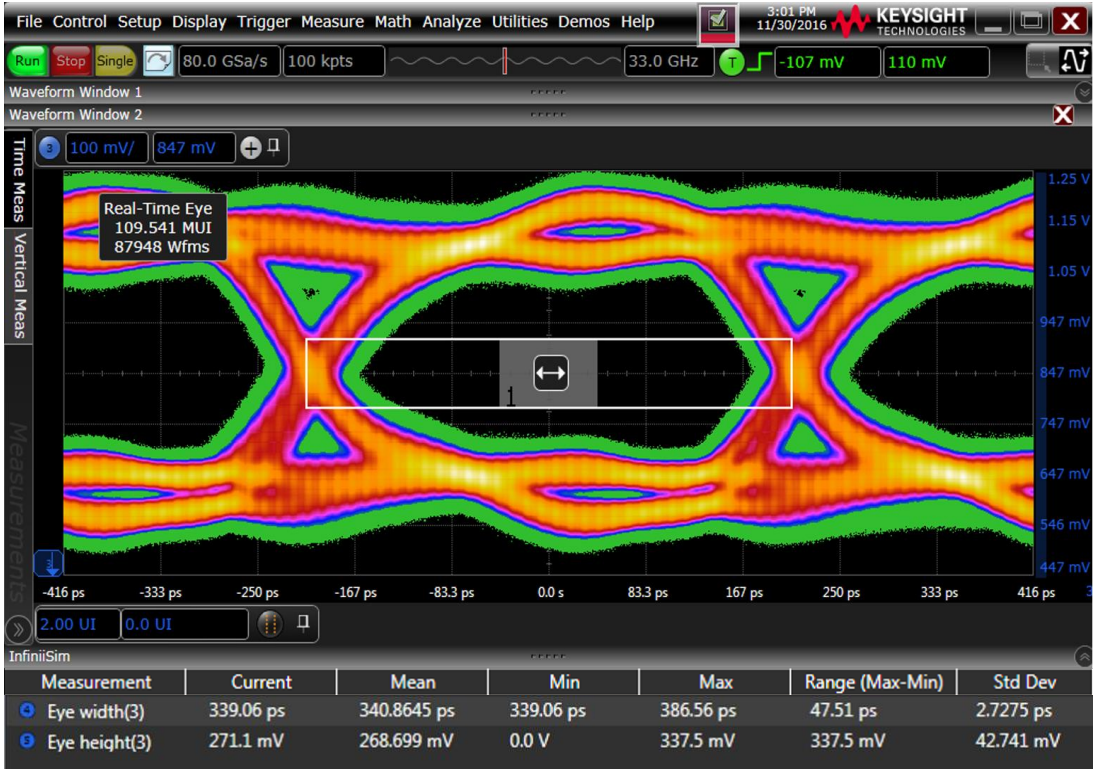




Measured Data

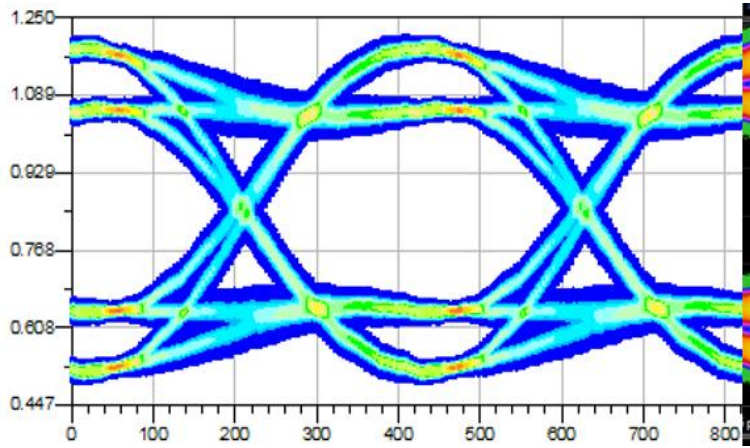
- **Measurement at 109million bits:**
  - Eye Width – 339 ps
  - Eye Height – 271 mV

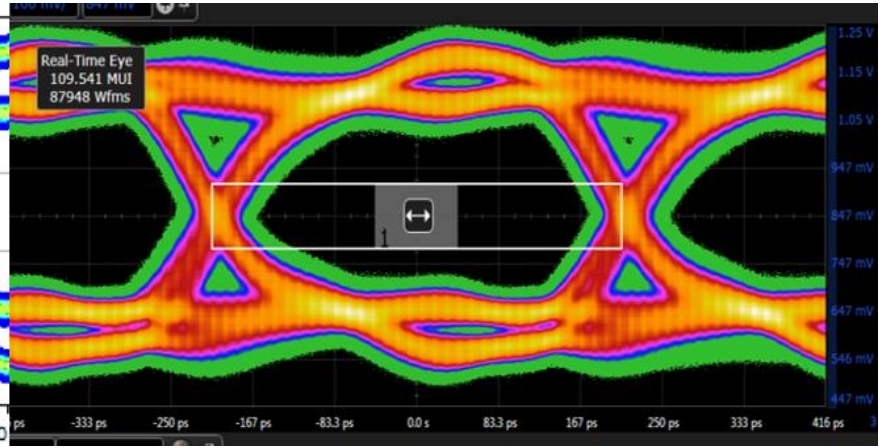
	Measurement Result (@1E^{-8} BER)
Eye Width	339 ps
Eye Height	271 mv



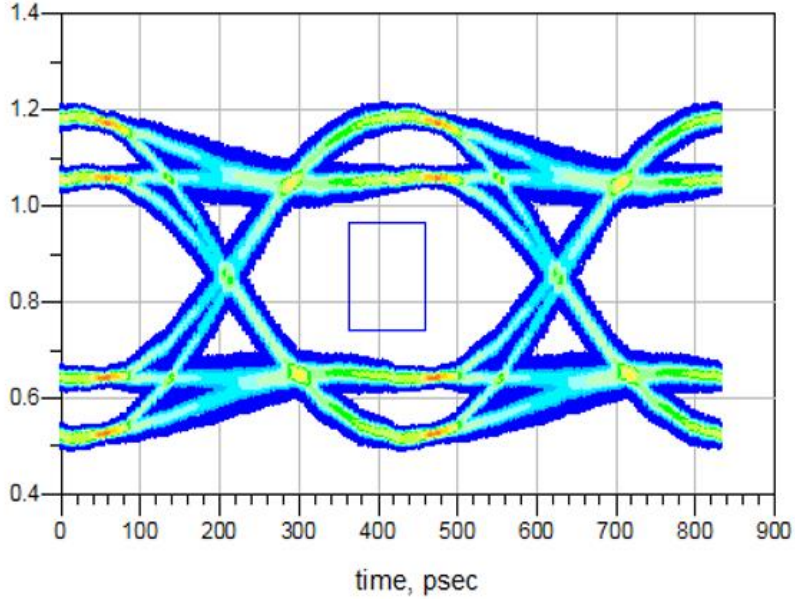
Side-By-Side Comparison

- **Statistical analysis vs. measured comparison on DQ35 – No correction:**
  - Reasonable agreement
  - Larger amplitude and jitter noise with the measured data due to the delta-I noise contribution





Corrected Mask – Still Within Spec!



measurement	Summary
WidthAtBER	3.229E-10
HeightAtBER	0.360
TimingMarginUL	6.771E-11
TimingMarginUR	6.354E-11
TimingMarginLL	6.354E-11
TimingMarginLR	6.354E-11
VoltageMarginUL	0.028
VoltageMarginUR	0.065
VoltageMarginLL	0.034
VoltageMarginLR	0.071
MinVoltageMarginU	0.028
MinVoltageMarginL	0.034

Amplitude MCF	Jitter MCF
94 mV	16 ps

	DDR4 DQ Mask in JEDEC Spec	New DQ Mask After Correction factor
Eye Width	0.2 UI	0.23 UI
Eye Height	130 mv	224 mv

Eye Height and Width with MCF Applied

- **Excellent agreement :**
  - 2% eye width difference on simulation vs. measured @ $1e^{-8}$ BER
  - 2.2% eye height difference on simulation vs. measured @ $1e^{-8}$ BER

	DDR BUS Sim Result @ $1E^{-16}$ BER		DDR BUS Sim Result @ $1E^{-8}$ BER		Measurement Result (@$1E^{-8}$ BER)	Sim/Measure Difference
	W/O correction factor	With correction factor	W/O correction factor	With correction factor		
Eye Width	323 ps	307 ps	348 ps	332 ps	339 ps	2%
Eye Height	360 mv	266 mv	371 mv	277 mv	271 mv	2.2%

Compared

Conclusion

- **Statistical simulation approach must be used for DDR4 to get an ultra-low BER,1e^{-16}.**
- **Statistical simulation approach assumes the system to be linear, so the delta-I noise contribution for SSN is ignored**
- **Proposed solution using the mask correction factor (MCF) improves the accuracy of DDR4 statistical simulation by compensating the delta-I noise contribution**
- **Simulated results with MCF agree well to the measured data**

References

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Thank you!

QUESTIONS?