Versatile IO Circuit Schemes for LPDDR4 with 1.8mW/Gbps/pin Power Efficiency

Kyoung-Hoi Koo
Outline

• Introduction for LPDDR4
• Channel Sensitivity Analysis
• Backward Compatibility
• Summary
Rapid Technology Revolution

Robust I/O circuit scheme for world’s first over 1.6Gbps LPDDR3

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SAMSUNG
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Mobile DRAM Power Requirements

A great user experience requires great power efficiency

- Phones are targeting 10+ days of standby
- Tablets in ‘connected standby’ targeting 2+ weeks
- Ultrabooks require “always on, always connected” power state, <5 battery drain within 16 hours
- Memory consumers up to 30% of the system power in standby modes

Source: JEDEC, 2013

Active and Standby power are critical for mobile platforms
Low Power DRAM Bandwidth

- **LPDDR3(x64) BW target is 17 GB/s**
  - Evolutionary successor to LPDDR2
  - Data rate up to 2133Mbps DDR
- **Wide IO(x512) BW target is 17GB/s**
  - Limited performance scalability
  - Data rate up to 266Mbps SDR
- **LPDDR4(x64) BW target is 34GB/s**
  - Scalable performance
  - Data rate up to 4.2Gbps DDR
- **WIO2(x256) BW target is 34 GB/s**
  - Scalable performance
  - Stacked-die configuration(x512, 68GB/s)
  - Data rate up to 1066Mbps DDR

Source: JEDEC, 2013
## LPDDR4 vs. DDR4 Comparison

<table>
<thead>
<tr>
<th>Attribute</th>
<th>LPDDR4</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Target Market</td>
<td>Mobile Devices</td>
<td>Laptop, PC, Server</td>
</tr>
<tr>
<td>Die Architecture</td>
<td>2chX16</td>
<td>1chX16</td>
</tr>
<tr>
<td>IO Spec.</td>
<td>~350mV LVSTL</td>
<td>POD_12</td>
</tr>
<tr>
<td>DLL in Dram</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Termination</td>
<td>VSSQ</td>
<td>VDDQ</td>
</tr>
<tr>
<td>CI/O</td>
<td>&lt;1.0pF</td>
<td>&gt;1.0pF</td>
</tr>
<tr>
<td>C/A</td>
<td>6pin SDR CA bus</td>
<td>22pins</td>
</tr>
<tr>
<td>Topology</td>
<td>Point-to-point PoP&amp;MCP</td>
<td>DIMM</td>
</tr>
<tr>
<td>Max. Frequency</td>
<td>3.2Gbps/4.2Gbps</td>
<td>3.2Gbps</td>
</tr>
<tr>
<td>Low Frequency operation</td>
<td>Yes</td>
<td>Yes (DLL off &lt;125MHz)</td>
</tr>
<tr>
<td>Target Supply</td>
<td>1.1V(1.0V)</td>
<td>1.2V</td>
</tr>
</tbody>
</table>

Source: JEDEC, 2013
Signaling Difference (LP3 vs. LP4)

LPDDR3 Signaling

LPDDR4 Signaling
LVSTL Signaling Level

Pull-up drive case

\[ I_{PU} = k(VDDQ - V_{th})^r \]

\[ V_{OH} = VDDQ - V_{th} \text{ (w/o } R_{TERM}) \]

\[ V_{OH} = I_{PU}R_{TERM} = VDDQ / 3 \text{ or } VDDQ / 2.5 \]

\[ V_{ref} = 0.5 \times V_{OH} \]

Pull-down drive case

\[ I_{R} = \frac{V_{OH}}{R_{TERM}} \]

\[ V_{OH} = I_{PU}R_{TERM} = VDDQ / 3 \text{ or } VDDQ / 2.5 \]

\[ V_{ref} = 0.5 \times V_{OH} \]
Driver Scheme for Ultra Low Ci/o

- Receiver end Cap. causes signal distortion
- Ci/o portion
  - Driver: ~40%
  - Receiver: ~5%
  - ESD: ~30%
  - Parasitic: ~25%
- Low Ci/o driver scheme
  - Pull-up unit: Voh level
  - Pull-down unit: slew-rate
- Target Ci/o value: 0.5~0.7pF
Special pre-driver/driver Control Scheme

- Proposed scheme for duty balance and minimized SSON
  - Independent pull-up and pull-down control
Fast Boost Reference Generator

- A wide range reference generator is required to support
  - w/o Voh calibration, w/ Voh calibration, un-termination mode
- Fast setting time for reference voltage change

<table>
<thead>
<tr>
<th>$V_{OH}$</th>
<th>Boundary</th>
<th>$V_{DDQ}=1.1V$</th>
<th>$V_{DDQ}=1.0V$</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DDQ}/3$</td>
<td>-15%</td>
<td>0.156</td>
<td>0.142</td>
<td>w/ $V_{OH}$ calibration</td>
</tr>
<tr>
<td></td>
<td>15%</td>
<td>0.211</td>
<td>0.192</td>
<td>w/ $V_{OH}$ calibration</td>
</tr>
<tr>
<td>$V_{DDQ}/2.5$</td>
<td>-15%</td>
<td>0.187</td>
<td>0.170</td>
<td>w/ $V_{OH}$ calibration</td>
</tr>
<tr>
<td></td>
<td>15%</td>
<td>0.253</td>
<td>0.230</td>
<td>w/ $V_{OH}$ calibration</td>
</tr>
<tr>
<td>$V_{DDQ}/3$</td>
<td>-30%</td>
<td>0.128</td>
<td>0.117</td>
<td>w/o $V_{OH}$ calibration</td>
</tr>
<tr>
<td></td>
<td>30%</td>
<td>0.238</td>
<td>0.217</td>
<td>w/o $V_{OH}$ calibration</td>
</tr>
<tr>
<td>$V_{DDQ}/2.5$</td>
<td>-30%</td>
<td>0.154</td>
<td>0.140</td>
<td>w/o $V_{OH}$ calibration</td>
</tr>
<tr>
<td></td>
<td>30%</td>
<td>0.286</td>
<td>0.260</td>
<td>Un-Termination</td>
</tr>
<tr>
<td>$V_{DDQ}-55$</td>
<td>$V_{DDQ}-0.55$</td>
<td>0.275</td>
<td>0.225</td>
<td></td>
</tr>
<tr>
<td>$V_{DDQ}-15$</td>
<td>$V_{DDQ}-0.15$</td>
<td>0.475</td>
<td>0.425</td>
<td></td>
</tr>
</tbody>
</table>
Calibration Circuit

- A wide range reference generator is required to support:
  - w/o Voh calibration, w/ Voh calibration, un-termination mode
- Fast setting time for reference voltage change
- Short calibration time for on-time P/V/T variation tracking

![Diagram of Calibration Circuit](image)

- 240ohm resistance
- Pull-down Array
- Pull-up Array
- FSM
- VDDQ
- *VREF
- calibrated code for VOH
- calibrated code for VSSQ-TERM

1st calibration-loop
2nd calibration-loop
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Channel Sensitivity Analysis

- Channel sensitivity analysis using DOE
- PKG length and Ci/o are most sensitive design parameters
• Considering power consumption weak ODT, low Ci/o is recommend
On-die De-cap. Estimation

- Cost effective on-die de-cap estimation method is required
Lower VDDQ Voltage Operation

- For ultra low power consumption, lower VDDQ voltage operation should be verified
  - ~4% timing margin degradation is expected under 1.0V conditions
  - Short channel length (AP-Memory) is required to ensure more timing margin
Case Study for PKG. Spacing

- Wider AP PKG. spacing securing ~14% eye-opening
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Signaling Features (LP3 vs. LP4)

LPDDR3 Signaling:
- PMOS pull-up: large pre-driver size
- VDDQ Termination
- Large swing
- Large current consumption
- Large SSN & X-talk

LPDDR4 Signaling:
- NMOS pull-up: small pre-driver size
- VOH_{max} = VDDQ - V_{th}
- VOH = Ipu \times R_{term}
- Reduced Cio
- Small swing, small SSN & X-talk
How to Combine LP3/LP4 Driver

- Change the VDDQ level?
- Performance degradation
- Mismatch in signaling level

- Change the pull-up driver?
- Area overhead
- Ci/o increase
## Proposed LP3/LP4 Driver Schemes

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Type A</th>
<th>Type B</th>
<th>Type C</th>
<th>Type D</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="Proposed_LP3_LP4_Driver_Schemes.png" alt="Diagram" /></td>
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</tr>
</tbody>
</table>

### Performance
- Pull-up/down matching: ☑️ ☑️ ☑️ ☑️
- CI/o: ☑️ ☑️ ☑️ ☑️

### Power
- Dynamic: ☑️ ☑️ ☑️ ☑️
- Static: ☑️ ☑️ ☑️ ☑️
- Leakage: ☑️ ☑️ ☑️ ☑️

### Area
- Driver: ☑️ ☑️ ☑️ ☑️

### Cost
- ☑️ ☑️ ☑️ ☑️
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Summary

• Versatile schemes for 3.2Gbps LPDDR4 interface
  – Ultra low (0.5~0.7pF) Ci/o driver scheme
  – Special pre-driver/driver control scheme
  – Internal Vref. generation with fast boost
  – VSSQ-TERM and Voh calibration

• Channel sensitivity analysis
  – DOE analysis
  – On-die de-cap. estimation
  – Lower VDDQ operation
  – AP PKG. spacing study
• Backward Compatibility
  – Differentiated MKT. solution for controller side
  – Proposed LP3/LP4 compatible driver scheme