DesignCon® 2014

Versatile IO Circuit Schemes for LPDDR4 with 1.8mW/Gbps/pin Power Efficiency

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UBM Tech

Outline

- Introduction for LPDDR4
- Channel Sensitivity Analysis
- Backward Compatibility
- Summary

Rapid Technology Revolution

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- Channel Sensitivity Analysis
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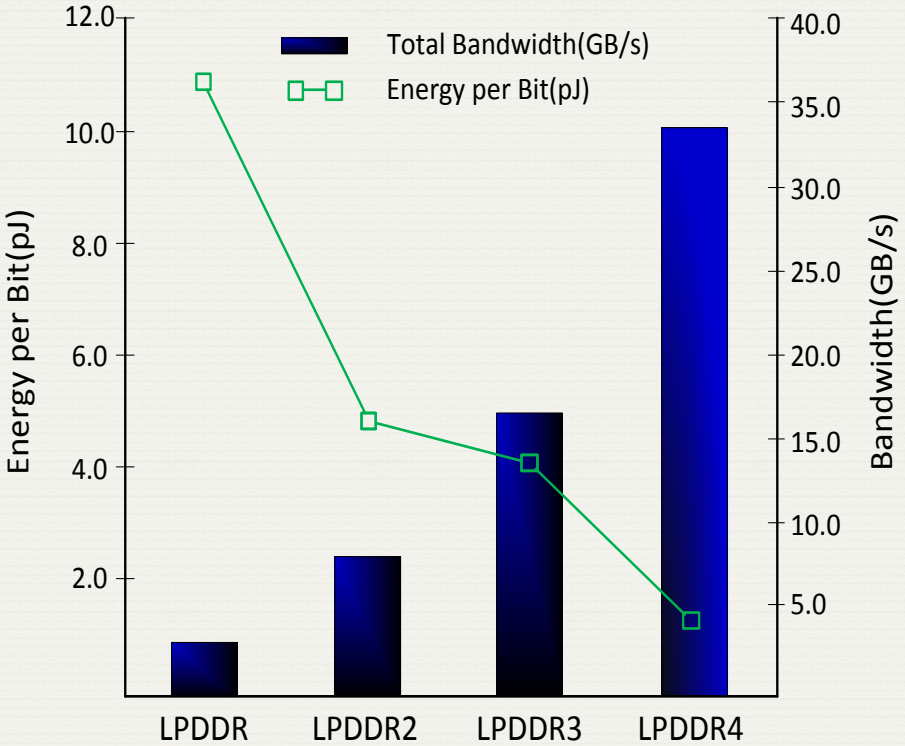
Mobile DRAM Power Requirements

A great user experience requires great power efficiency

- Phones are targeting 10+ days of standby
- Tablets in 'connected standby' targeting 2+ weeks
- Ultrabooks require "always on, always connected" power state,<5 battery drain within 16 hours
- Memory consumers up to 30% of the system power in standby modes

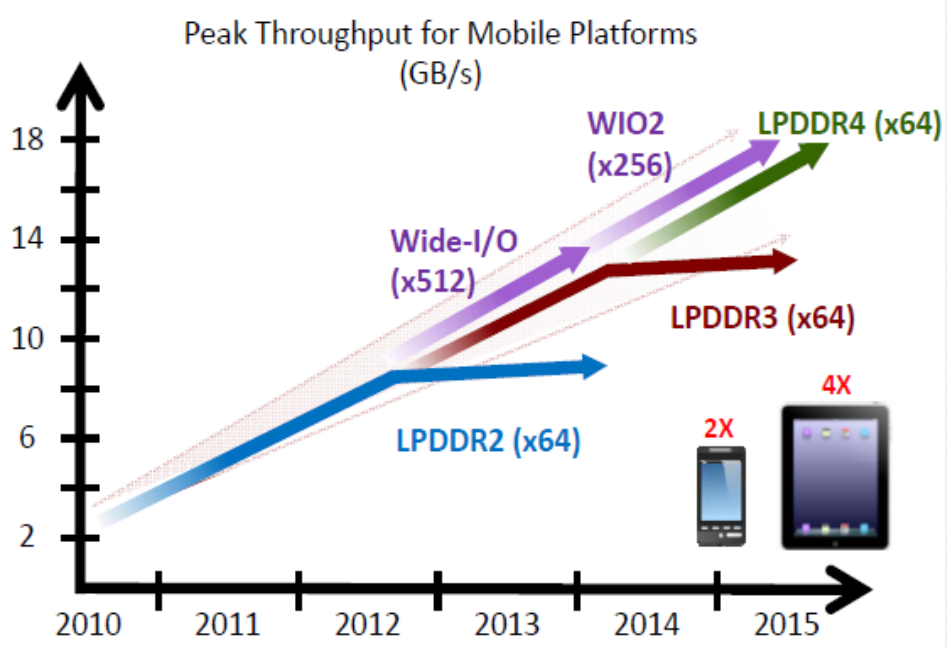


Source : JEDEC, 2013

Active and Standby power are critical for mobile platforms

Low Power DRAM Bandwidth

- LPDDR3(x64) BW target is 17 GB/s
  - Evolutionary successor to LPDDR2
  - Data rate up to 2133Mbps DDR
- Wide IO(x512) BW target is 17GB/s
  - Limited performance scalability
  - Data rate up to 266Mbps SDR
- LPDDR4(x64) BW target is 34GB/s
  - Scalable performance
  - Data rate up to 4.2Gbps DDR
- WIO2(x256) BW target is 34 GB/s
  - Scalable performance
  - Stacked-die configuration(x512, 68GB/s)
  - Data rate up to 1066Mbps DDR



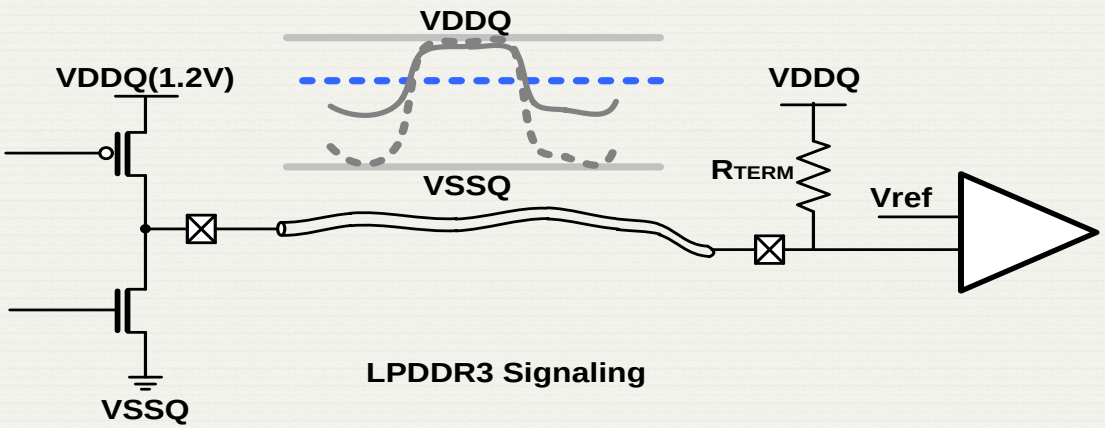
Source : JEDEC, 2013

LPDDR4 vs. DDR4 Comparison

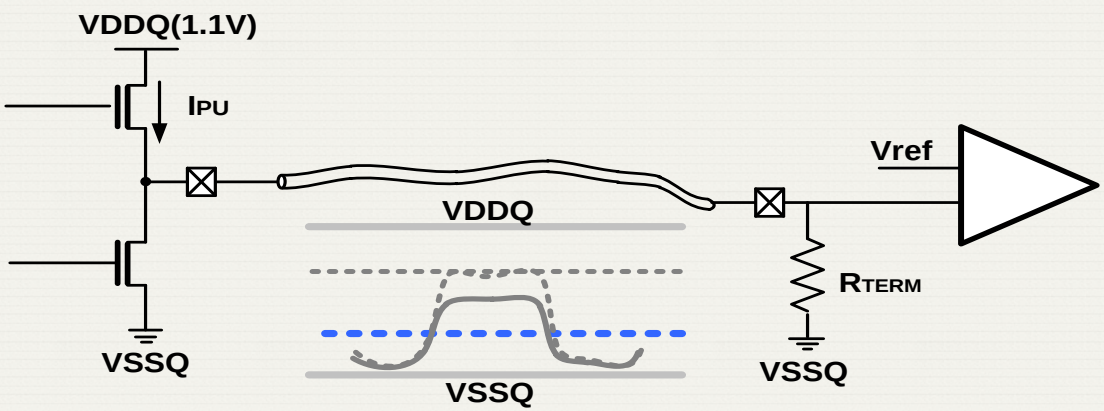
Source : JEDEC, 2013

Attribute	LPDDR4	DDR4
Target Market	Mobile Devices	Laptop,PC,Server
Die Architecture	2chX16	1chX16
IO Spec.	~350mV LVSTL	POD_12
DLL in Dram	No	Yes
Termination	VSSQ	VDDQ
CI/O	<1.0pF	>1.0pF
C/A	6pin SDR CA bus	22pins
Topology	Point-to-point PoP&MCP	DIMM
Max. Frequency	3.2Gbps/4.2Gbps	3.2Gbps
Low Frequency operation	Yes	Yes (DLL off <125MHz)
Target Supply	1.1V(1.0V)	1.2V

Signaling Difference(LP3 vs. LP4)



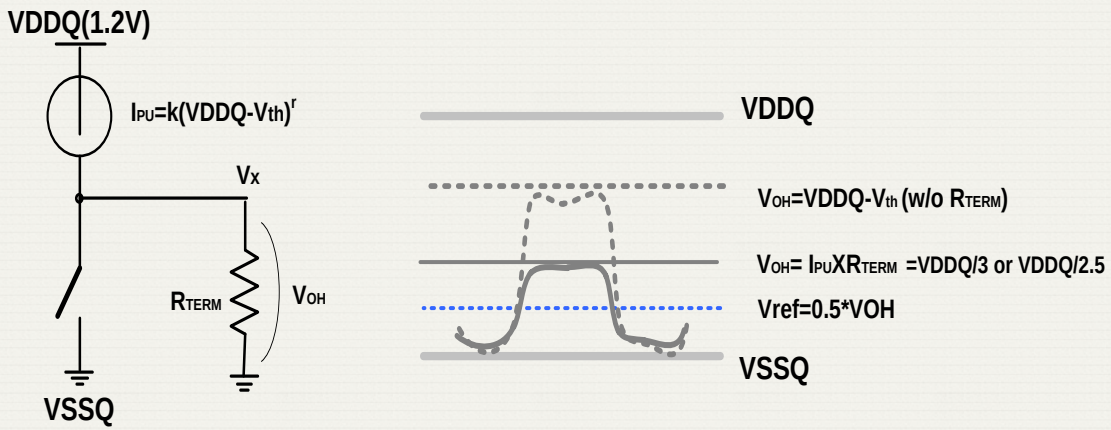
LPDDR3 Signaling



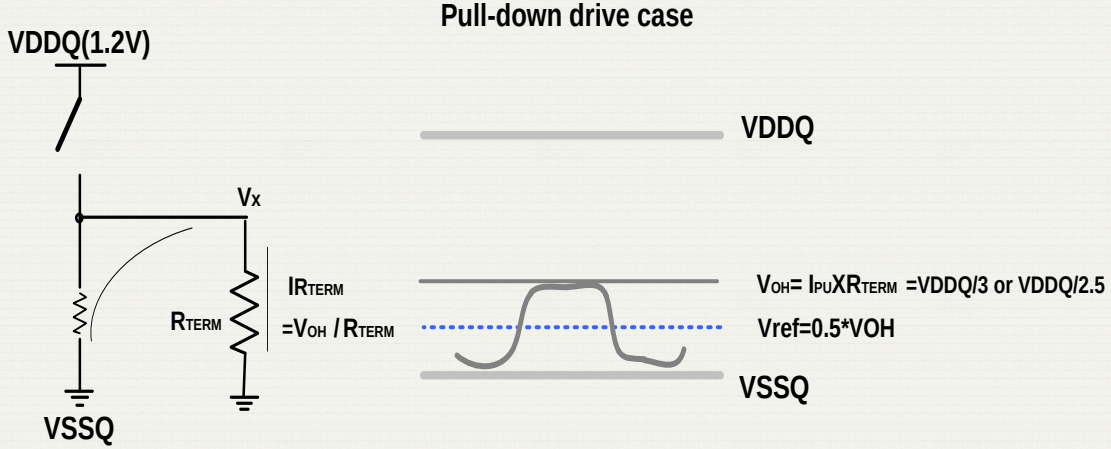
LPDDR4 Signaling

LVSTL Signaling Level

Pull-up drive case

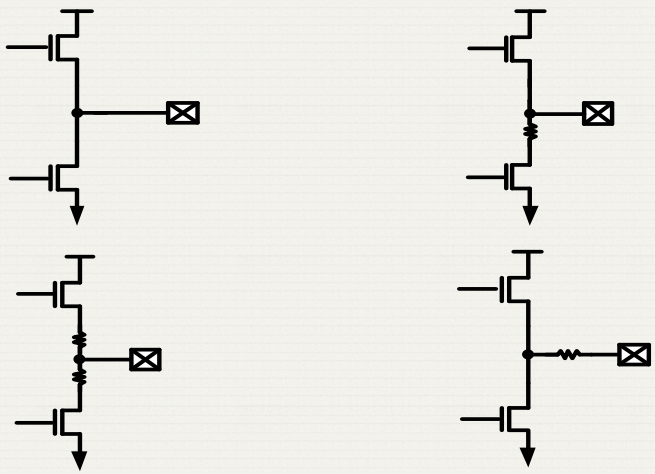


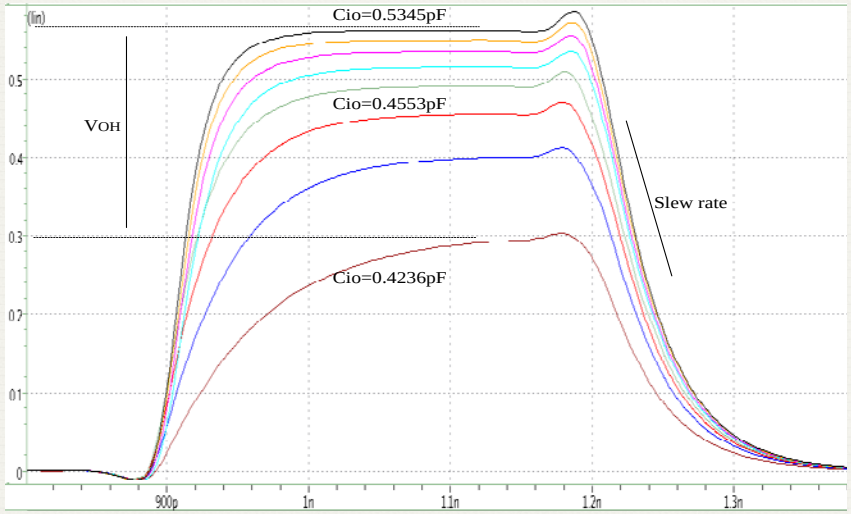
Pull-down drive case



Driver Scheme for Ultra Low Ci/o

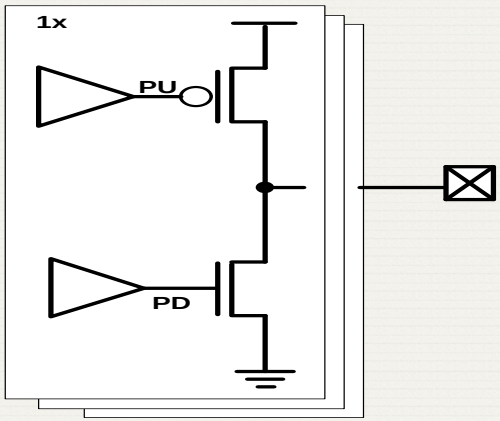
- Receiver end Cap. causes signal distortion
- Ci/o portion
  - Driver : ~40%
  - Receiver : ~5%
  - ESD : ~30%
  - Parasitic: ~25%
- Low Ci/o driver scheme
  - Pull-up unit : Voh level
  - Pull-down unit : slew-rate
- Target Ci/o value : 0.5~0.7pF



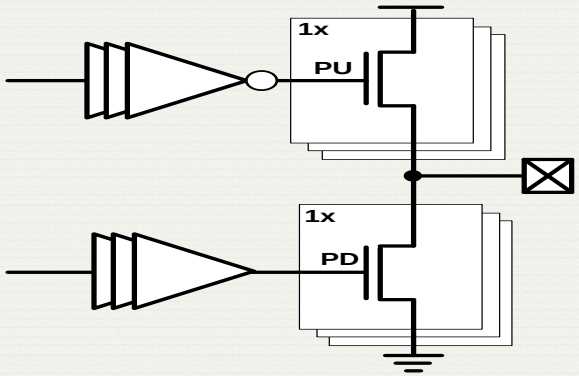


Special pre-driver/driver Control Scheme

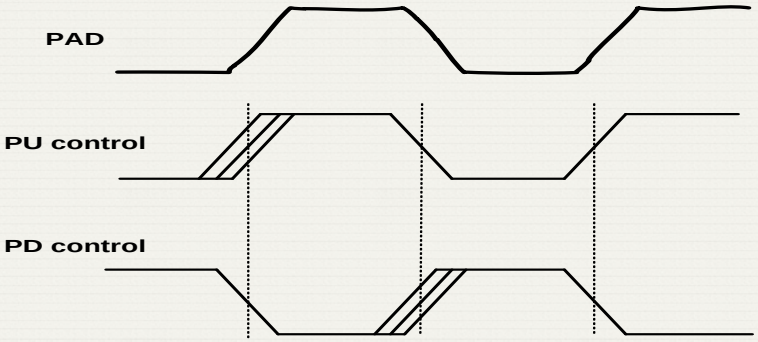
- Proposed scheme for duty balance and minimized SSON
  - Independent pull-up and pull-down control



Conventional scheme



Proposed scheme

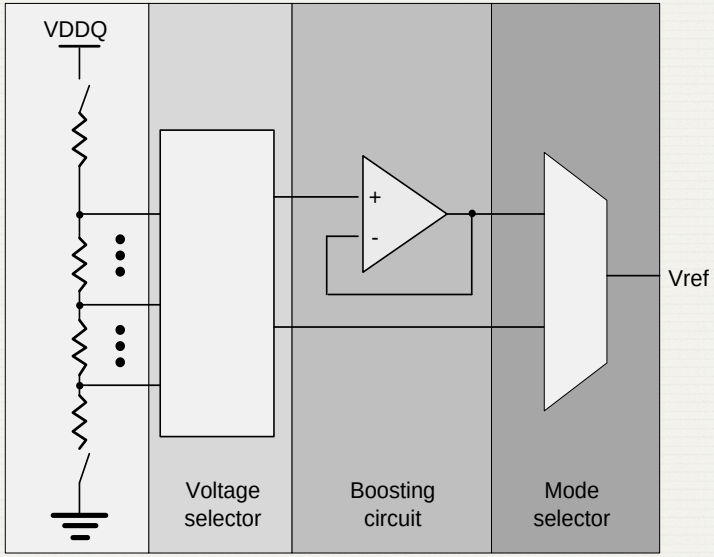


pre-driver control timing

Fast Boost Reference Generator

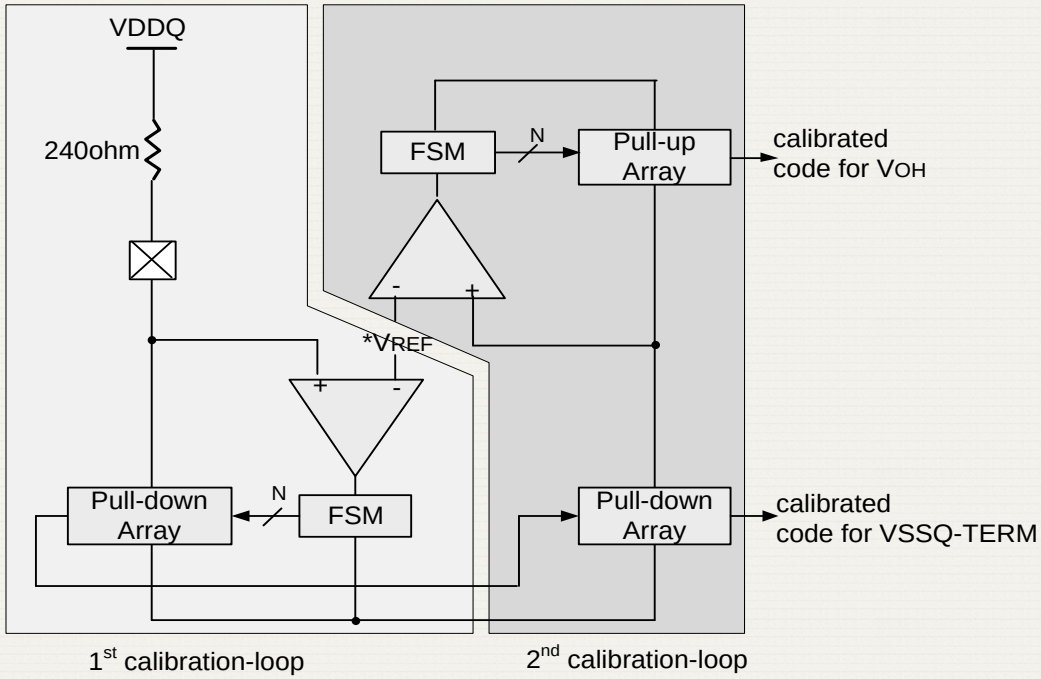
- A wide range reference generator is required to support
  - w/o Voh calibration, w/ Voh calibration, un-termination mode
- Fast setting time for reference voltage change

V_{OH}	Boundary	VDDQ=1.1V	VDDQ=1.0 V	Condition
		Vref	Vref	
VDDQ/3	-15%	0.156	0.142	w/ V_{OH} calibration
	15%	0.211	0.192	
VDDQ/2.5	-15%	0.187	0.170	
	15%	0.253	0.230	
VDDQ/3	-30%	0.128	**0.117**	w/o V_{OH} calibration
	30%	0.238	0.217	
VDDQ/2.5	-30%	0.154	0.140	
	30%	**0.286**	0.260	
VDDQ-55	VDDQ-0.55	0.275	0.225	Un-Termination
VDDQ-15	VDDQ-0.15	**0.475**	0.425	



Calibration Circuit

- A wide range reference generator is required to support
  - w/o Voh calibration, w/ Voh calibration, un-termination mode
- Fast setting time for reference voltage change
- Short calibration time for on-time P/V/T variation tracking



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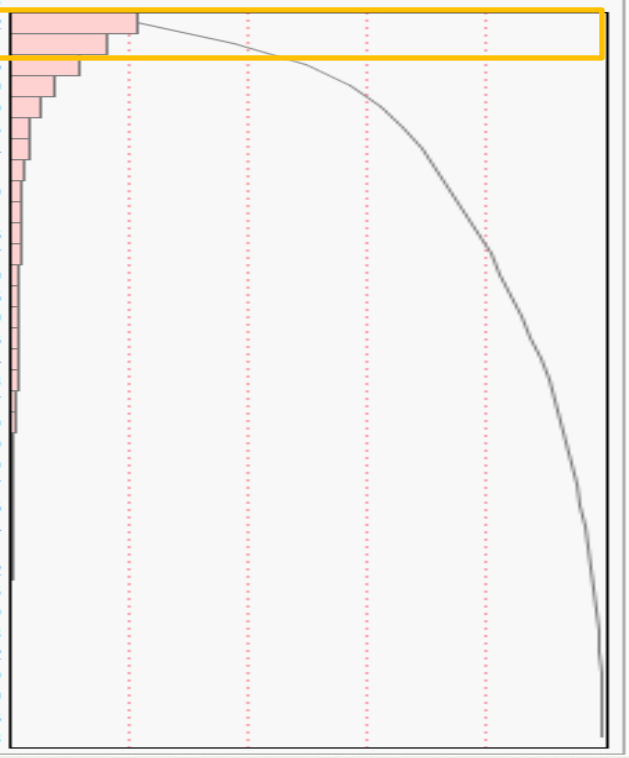
Channel Sensitivity Analysis

- Channel sensitivity analysis using DOE
- PKG length and Ci/o are most sensitive design parameters

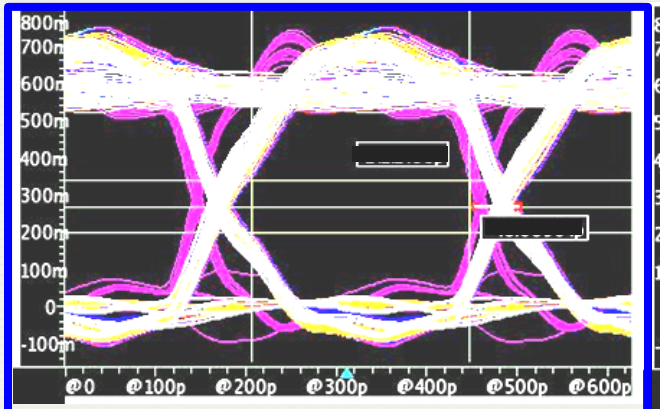
Pareto Plot of Transformed Estimates

Term	Orthog Estimate
apl	-20.71572
dram_cio	-15.89351
meml	-11.33885
cnr	7.18429
aps	5.00080
dram_rdie	-3.52276
(dram_cio-0.9)*(meml-6.02)	-3.15694
(odt-91.2)*(dram_rdie-18)	2.37371
(dram_cio-0.9)*(aps-22.725)	-2.22140
cnr*(odt-91.2)	-2.19051
cnr*(dram_cio-0.9)	-2.19043
(apl-4.04)*(aps-22.725)	1.91087
(odt-91.2)*(odt-91.2)	-1.73499
cnr*(apl-4.04)	-1.73085
(apl-4.04)*(meml-6.02)	-1.68259
(dram_cio-0.9)*(apl-4.04)	1.54133
odt	1.50264
(dram_cio-0.9)*(dram_cio-0.9)	1.36268
(dram_cio-0.9)*(dram_rdie-18)	1.03517
(meml-6.02)*(aps-22.725)	0.95010
(dram_rdie-18)*(aps-22.725)	-0.84730
(dram_rdie-18)*(apl-4.04)	0.75630
(meml-6.02)*(meml-6.02)	0.73167
(dram_rdie-18)*(meml-6.02)	-0.70155
cnr*(aps-22.725)	0.62774
cnr*(meml-6.02)	0.56611
(odt-91.2)*(apl-4.04)	-0.53712
cnr*cnr	0.40606
(odt-91.2)*(dram_cio-0.9)	-0.36570
(aps-22.725)*(aps-22.725)	0.33848
cnr*(dram_rdie-18)	0.33222
(odt-91.2)*(aps-22.725)	0.28840
(dram_rdie-18)*(dram_rdie-18)	0.19899
(apl-4.04)*(apl-4.04)	-0.05933
(odt-91.2)*(meml-6.02)	0.00258

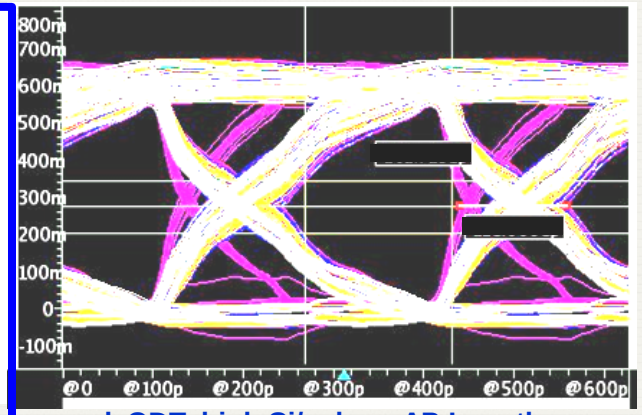


Channel Sensitivity Analysis-cont.

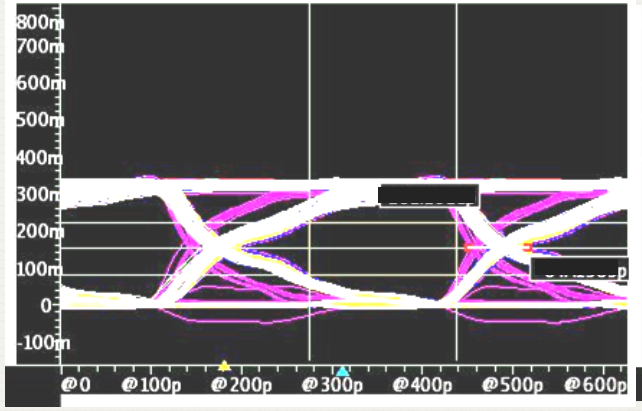
- Considering power consumption weak ODT, low Ci/o is recommend



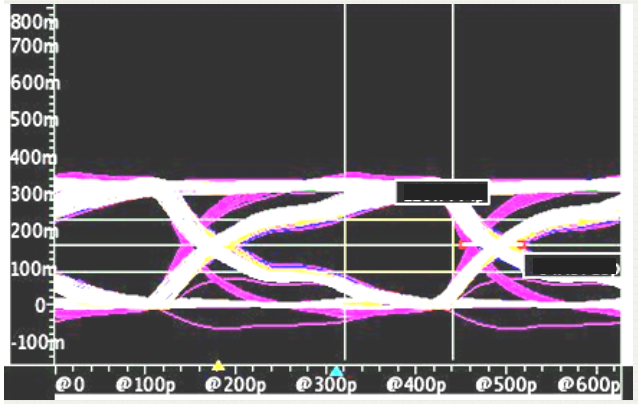
weak ODT, low Ci/o, short AP Length



weak ODT, high Ci/o, long AP Length



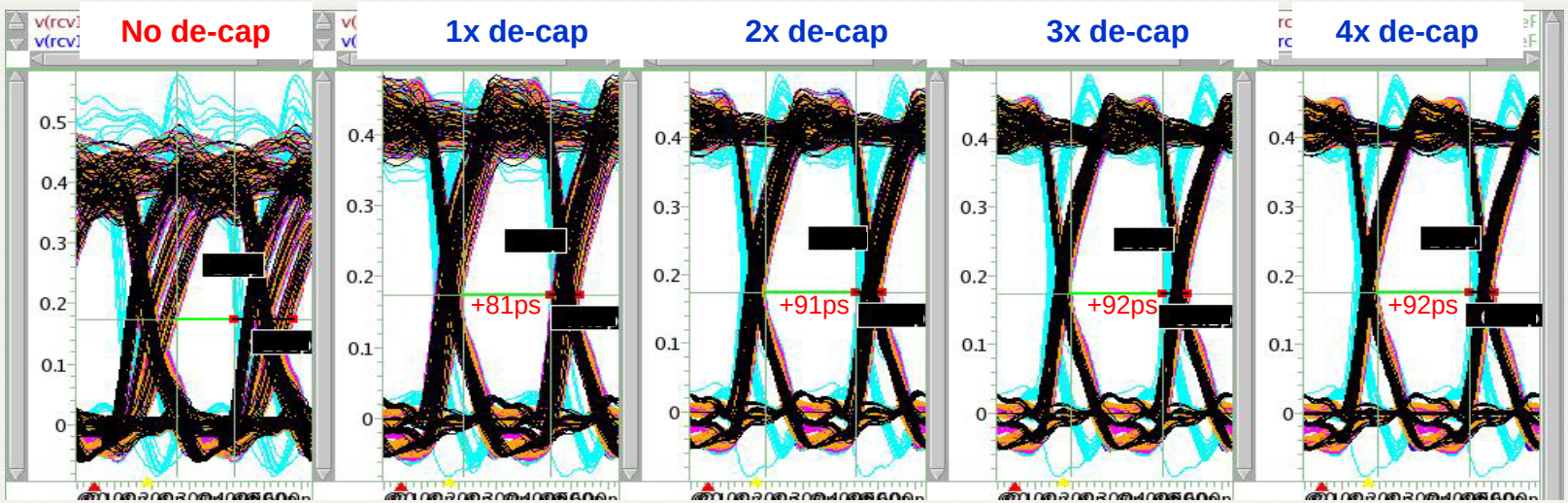
strong ODT, low Ci/o, short AP Length

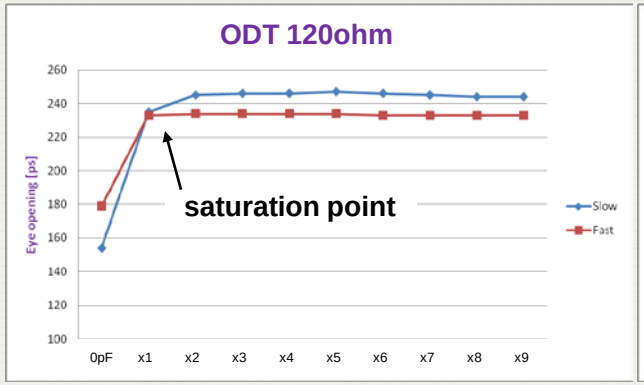


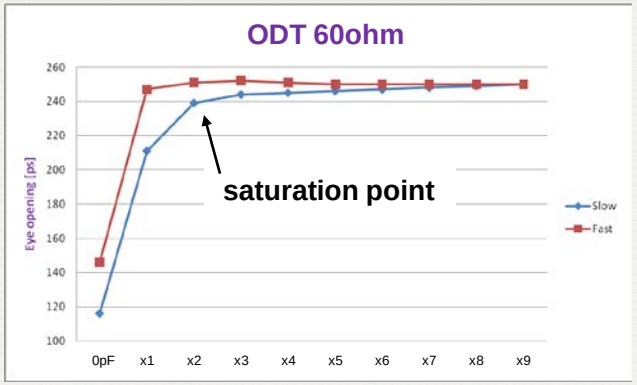
strong ODT, high Ci/o, long AP Length

On-die De-cap. Estimation

- Cost effective on-die de-cap estimation method is required

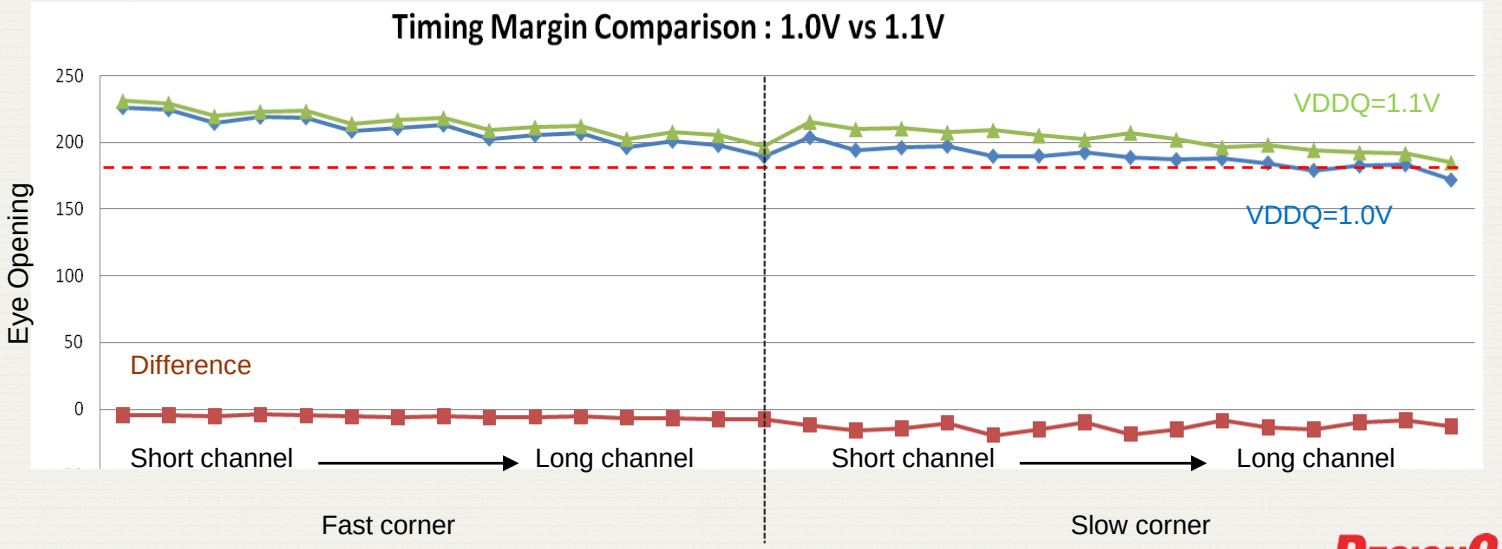






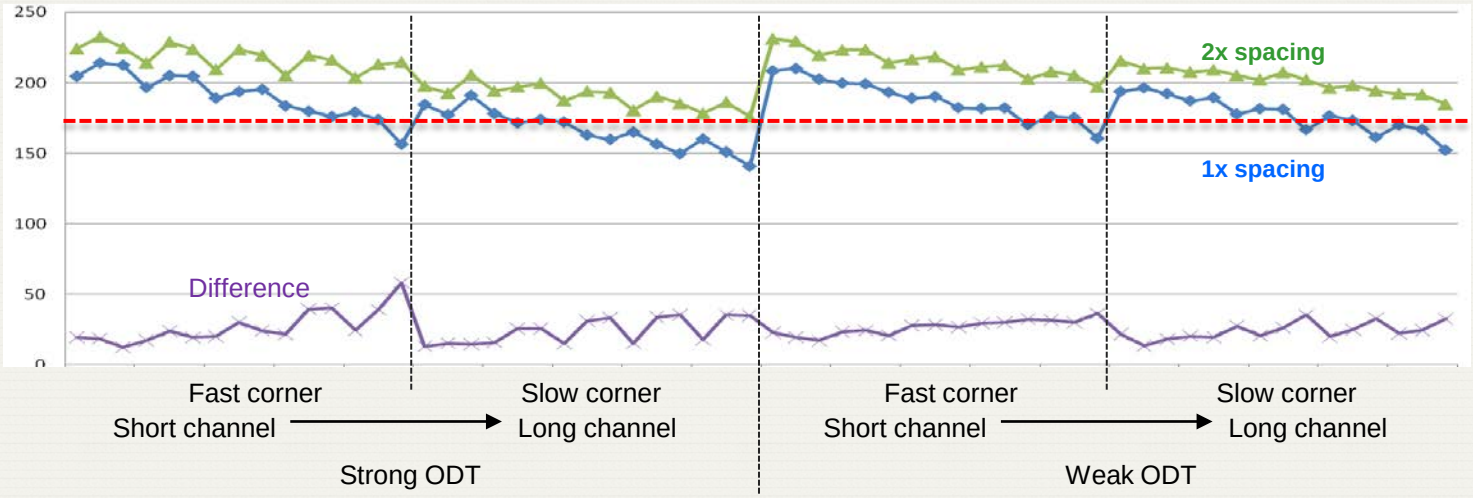
Lower VDDQ Voltage Operation

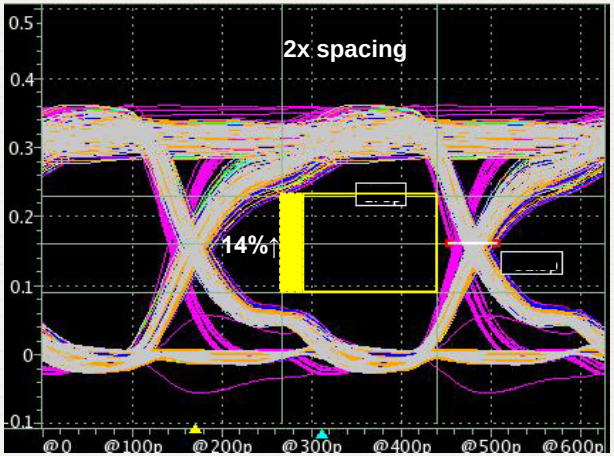
- For ultra low power consumption, lower VDDQ voltage operation should be verified
  - ~4% timing margin degradation is expected under 1.0V conditions
  - Short channel length (AP-Memory) is required to ensure more timing margin

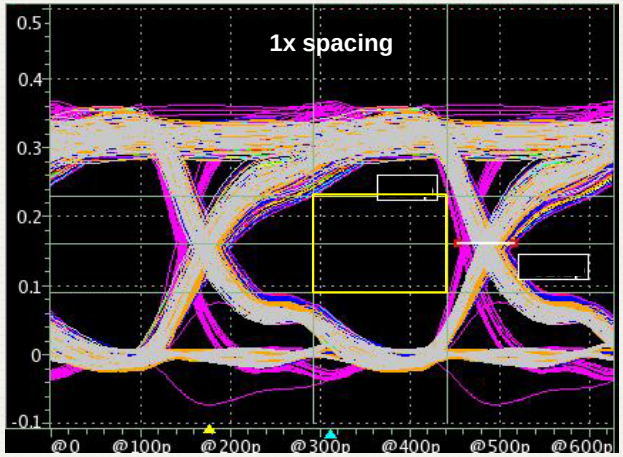


Case Study for PKG. Spacing

- Wider AP PKG. spacing securing ~14% eye-opening







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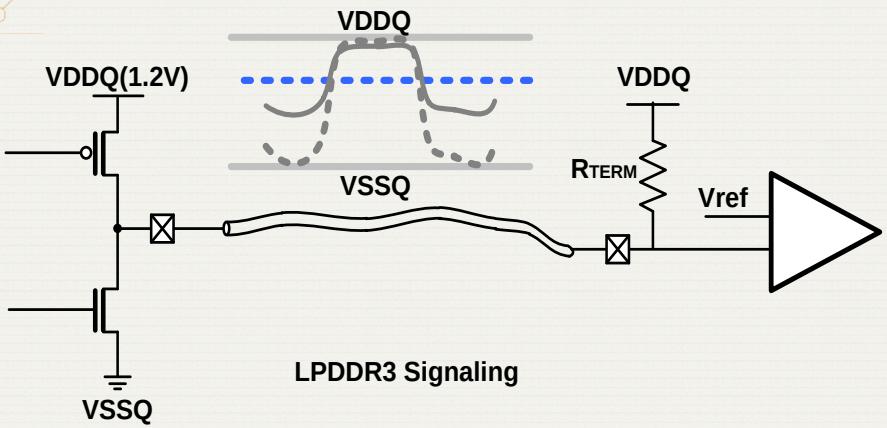
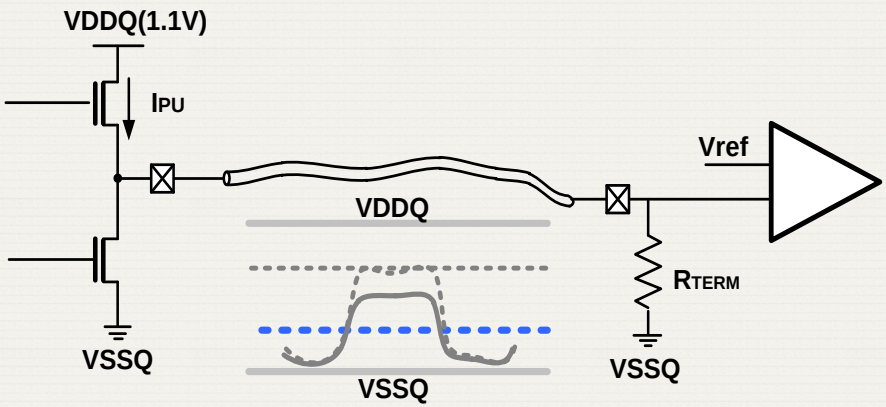
Signaling Features(LP3 vs. LP4)



LPDDR3 Signaling

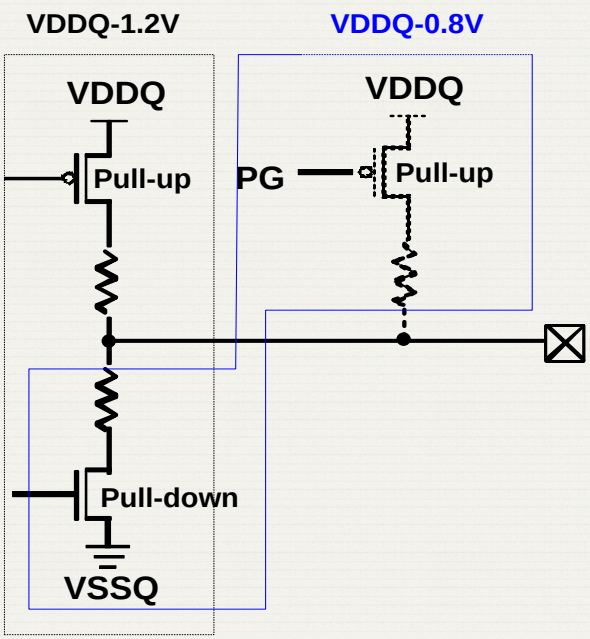
- ✓ PMOS pull-up : large pre-driver size
- ✓ VDDQ Termination
- ✓ Large swing
- ✓ Large current consumption
- ✓ Large SSN & X-talk

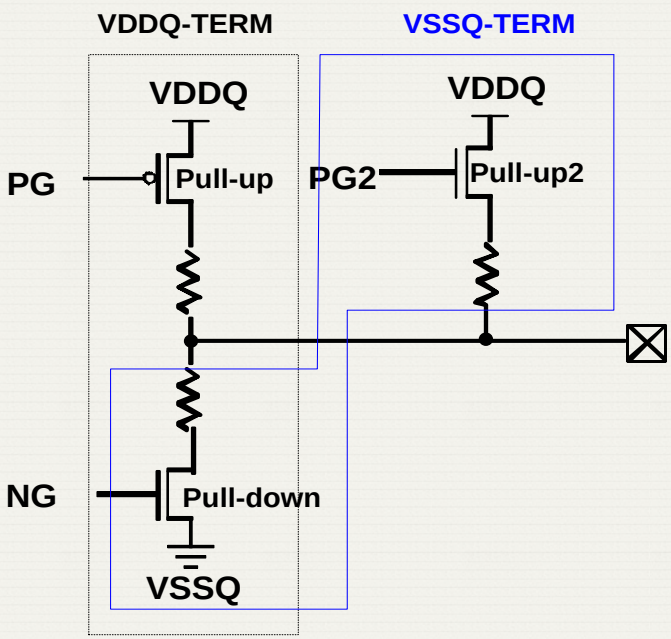


LPDDR4 Signaling

- ✓ NMOS pull-up : small pre-driver size
- ✓ VOHmax=VDDQ-Vth
- ✓ VOH=Ipu*Rterm
- ✓ Reduced Cio
- ✓ Small swing, small SSN & X-talk

How to Combine LP3/LP4 Driver

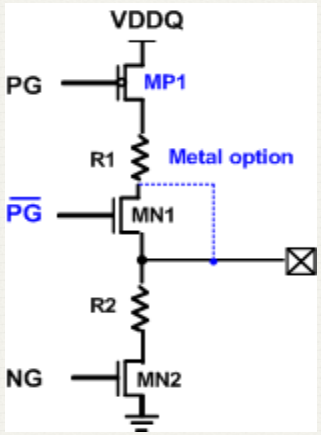
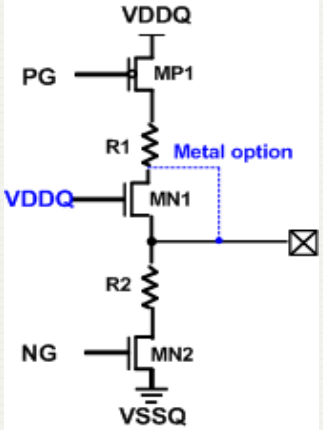
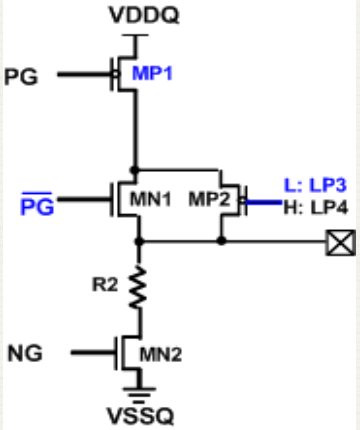
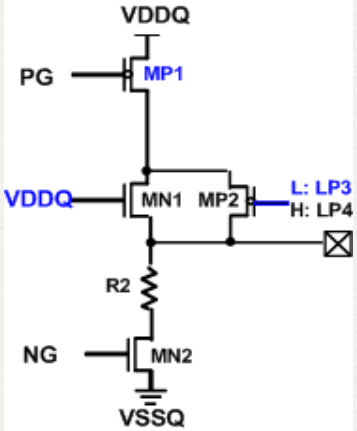




- ✓ Change the VDDQ level?
- ✓ Performance degradation
- ✓ Mismatch in signaling level

- ✓ Change the pull-up driver?
- ✓ Area overhead
- ✓ Ci/o increase

Proposed LP3/LP4 Driver Schemes

		Type A	Type B	Type C	Type D
Scheme					
Performance	Pull-up/down matching	☺☺	☺☺	☺	☺
	Ci/o	☺☺☺	☺☺	☺	☺
Power	Dynamic	☺	☺☺	☺	☺☺
	Static	☺☺	☺☺	☺	☺
	Leakage	☺☺	☺☺	☺	☺
Area	Driver	☺	☺☺☺	☺	☺☺
Cost		☺	☺	☺☺☺	☺☺☺

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Summary

- Versatile schemes for 3.2Gbps LPDDR4 interface
  - Ultra low(0.5~0.7pF) Ci/o driver scheme
  - Special pre-driver/driver control scheme
  - Internal Vref. generation with fast boost
  - VSSQ-TERM and Voh calibration
- Channel sensitivity analysis
  - DOE analysis
  - On-die de-cap. estimation
  - Lower VDDQ operation
  - AP PKG. spacing study

Summary-cont.

- Backward Compatibility
  - Differentiated MKT. solution for controller side
  - Proposed LP3/LP4 compatible driver scheme