Authors

▶ **Thomas To, Xilinx Inc.**

▶ **Penglin Niu, Xilinx Inc.**

▶ **Juan Wang, Xilinx Inc.**

▶ **Changyi Su, Xilinx Inc.**

▶ **Chong Ling Khoo, Xilinx Inc.**

▶ **Ajay Kumar Sharma, Xilinx Inc.**

▶ **Dmitry Klokotov, Xilinx Inc.**

▶ **Wei Liu, Xilinx Inc.**

▶ **Yong Wang, Xilinx Inc.**

FPGA High Speed High Bandwidth Unique Challenges

➤ **Massive amount of High Performance IO can be used for DDR4**

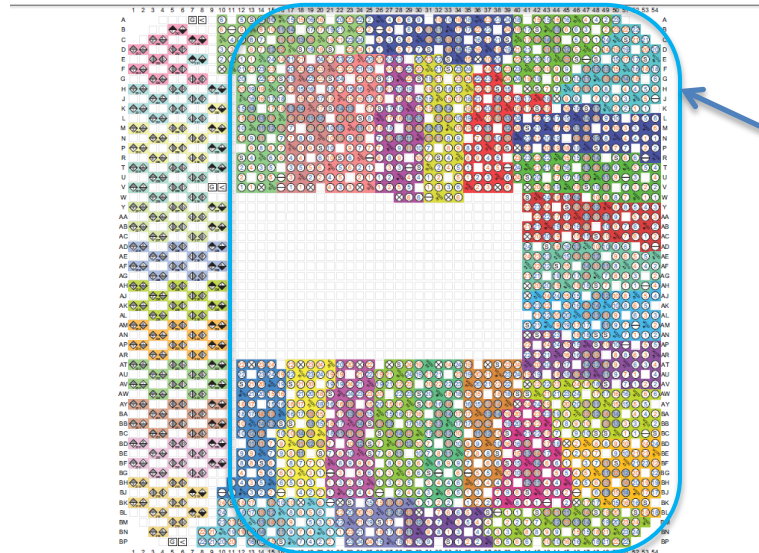|	KINTEX	KINTEX UltraSCALE	VIRTEX	VIRTEX UltraSCALE
Logic Cells (LC)	478	1,161	1,995	4,407
Block RAM (BRAM; Mbits)	34	76	68	115
DSP48	1,920	5,520	3,600	2,880
Peak DSP Performance (GMACs)	2,845	8,180	5,335	4,268
Transceiver Count	32	64	96	104
Peak Transceiver Line Rate (Gbps)	12.5	16.3	28.05	32.75
Peak Transceiver Bandwidth (Gbps)	800	2,086	2,784	5,101
PCI Express Blocks	1	6	4	6
100G Ethernet Blocks	-	1	-	7
150G Interlaken Blocks	-	2	-	9
Memory Interface Performance (Mbps)	1,866	2,400	1,866	2,400
I/O Pins	500	832	1,200	1,456

High Performance IO (HPIO) Support Many IO Standards

➤ **FPGA Programmable HPIO supports many memory /non memory interfaces.**

	IO Standards
DDR4	POD12
DDR3	SSTL15
DDR3L	SSTL135
LPDDR3	HSUL
RLDRAM3	SSTL12
QDR4	HSTL/SSTL:1.2V,1.25V POD:1.1V,1,2V
QDR2+	HSTL:1.2V,1.8V
LVDS	LVDS

➤ **Combo IO supports interfaces that have different electrical standards.**

   – Extra burden on FPGA IO

➤ **FPGA IO capacitance is much higher than in ASIC design.**

FPGA HP IO Package Pin Mapping

➤ **HP IOs are located at the center & around the package, IO breakouts are more susceptible to cross talk– XCVU440 FLGA2892**

HP IOs
1404 HPIO pins

Unique FPGA Challenges

➤ **High density IO Pin support many interfaces simultaneously.**

➤ **Highly programmable to customer requirements.**

➤ **Higher IO Capacitances than ASIC**
  - **FPGA IO Cap = 3.5pF versus Typical ASIC IO Cap =~1.0pF**
  - **Silicon timing uncertainty higher compared to ASIC**
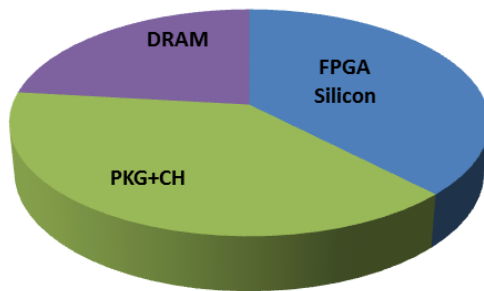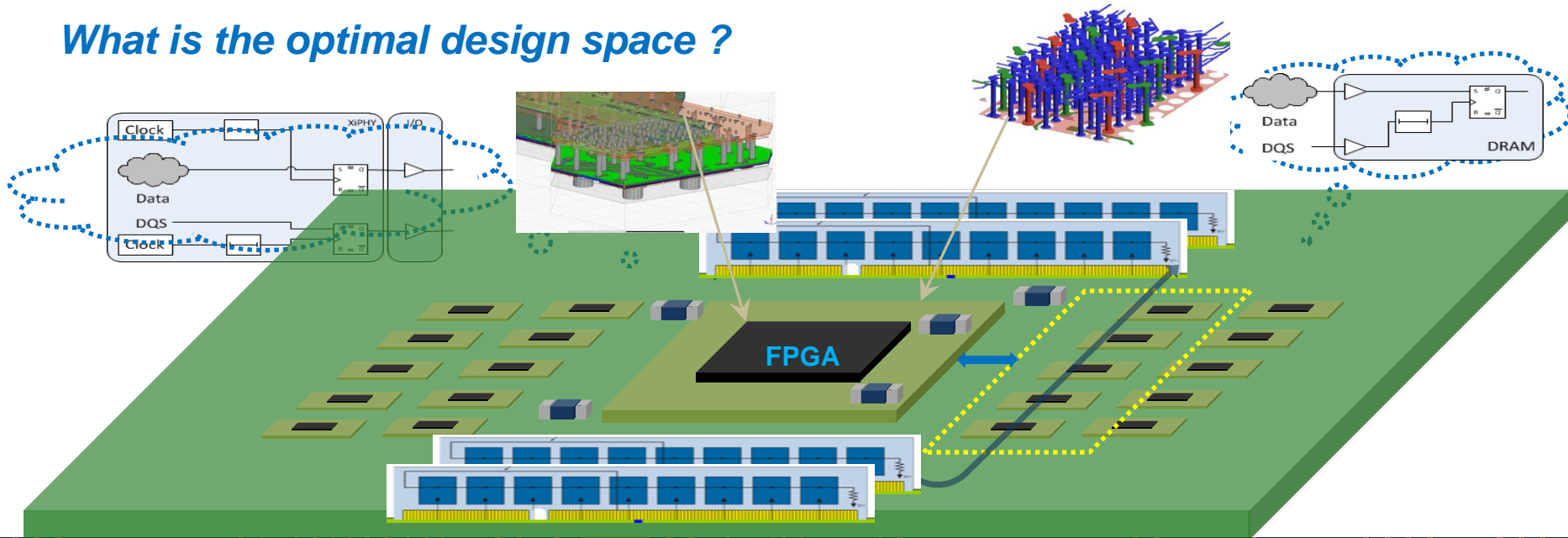

➤ **Lead to different design space & optimizations.**

#DC15

High Speed Parallel Bus System Considerations

What are the memory technologies to support & their speeds?

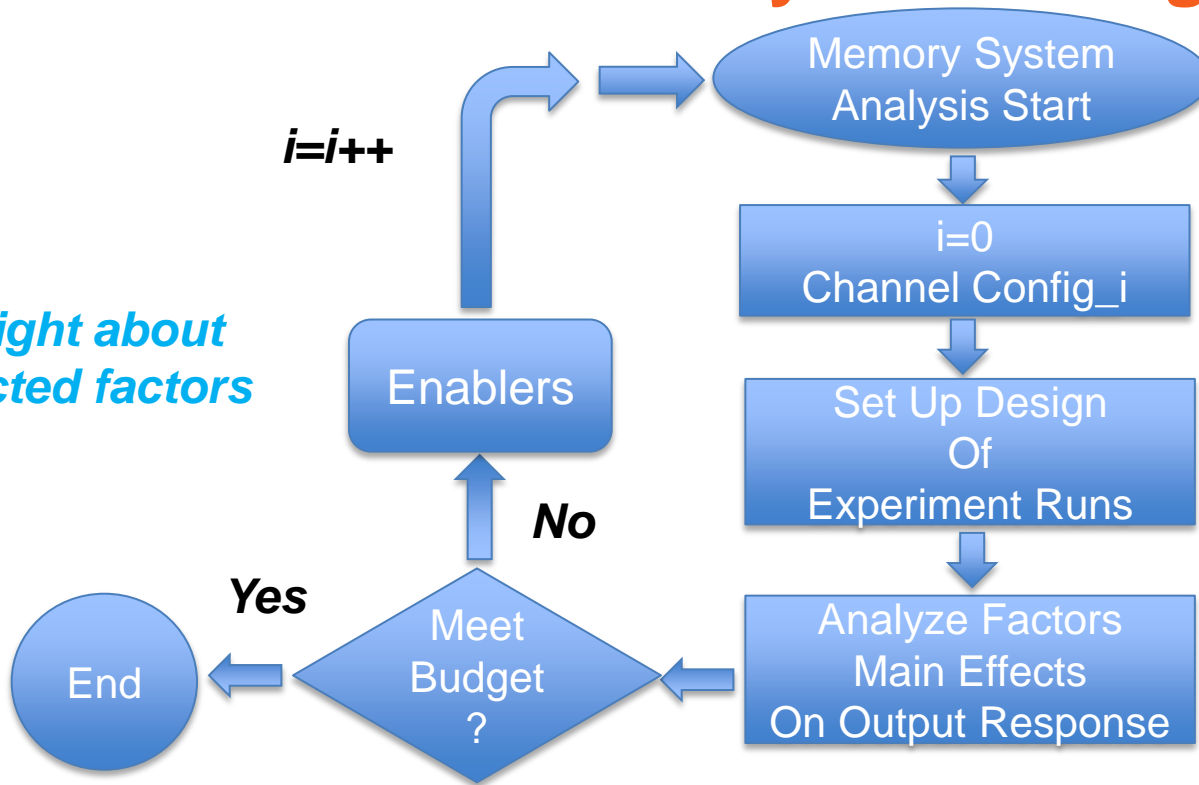*What are the memory devices variations & electrical limits?*

What are the electrical channel characteristics ?

What is the optimal design space ?

High Speed Parallel IO Bus System Design Flow

Statistical Design Of Experiment Approach

Identify the performance output (Response)
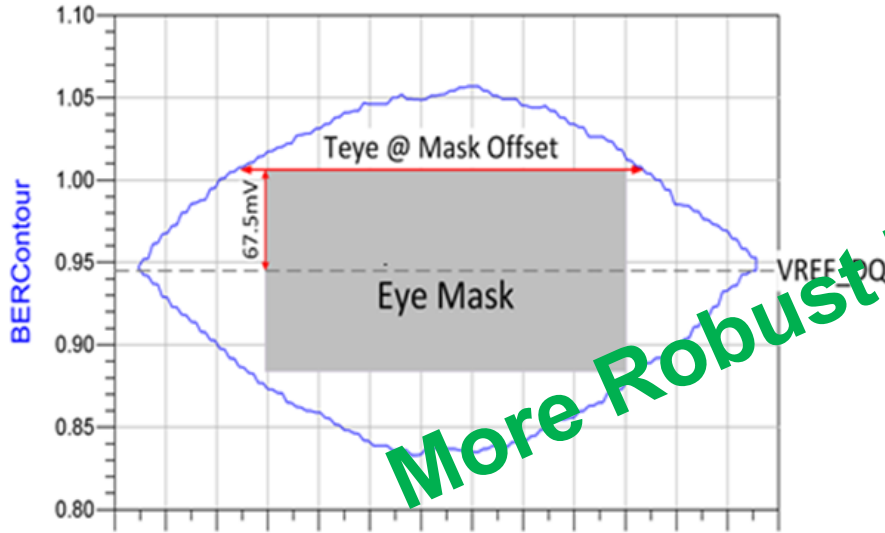
Identify the design factors (parameters) limits

Create design run table & simulate response(s)

Analyze response & Identify key design parameters from Prediction Profiles

Design Parameter Table & Design Data Eye Response

	Design Factors	Low Limits	Up Limit
FPGA	Drv Slew Rate (V/ns)	-1	+1
	Drv Impedance (Ω)	-1	+1
	Dr Supply (V)	-1	+1
Package	Impedance (Ω)	-1	+1
	: : :	: : :	: : :
	: : :	: : :	: : :
Board	Impedance (Ω)	-1	+1
	: : :	: : :	: : :
	: : :	: : :	: : :
DRAM	Dram Cap Load	-1	+1
	Rtt	-1	+1
	: : :	: : :	: : :

→ *Systematic approach provides solid understanding of critical design factors*

→ *Controllable critical factors can re-center their nominal values to maximize margin*

IO Key Features to Enable DDR4 Interface

➤ **Mother Board via Improvement Quantification**

 – Upper Routing vs Lower Routing improvement

➤ **Tx Feature**

 – POD12 Driver with De-emphasis Equalization

➤ **Rx Feature**

 – Continuous Time Linear Equalization

➤ **De-skew Feature**

 – Data (DQ) & Data Strobe (DQS) per bit de-skew

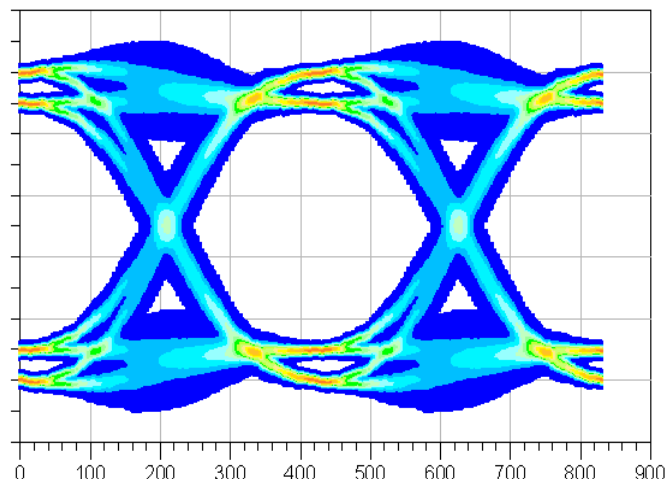# Mother Board Via Cross Talk Quantification
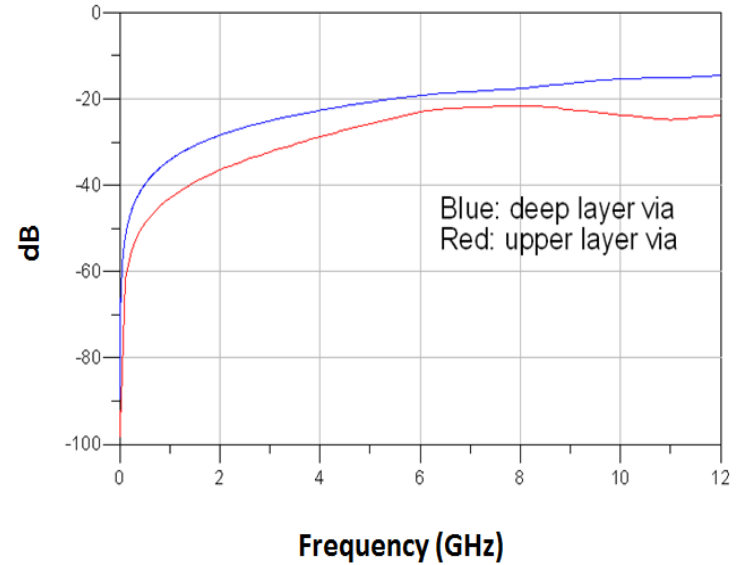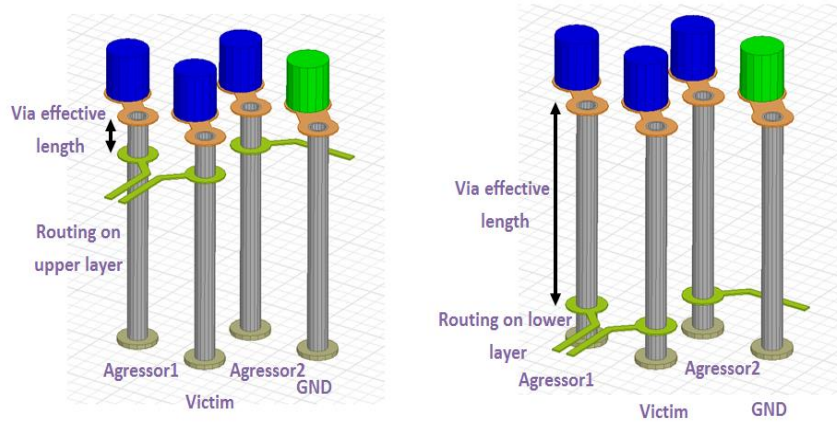
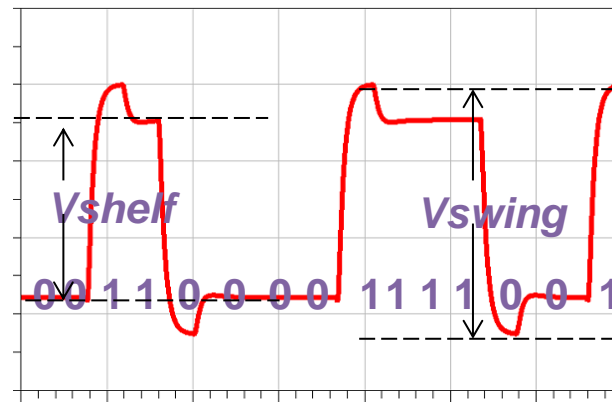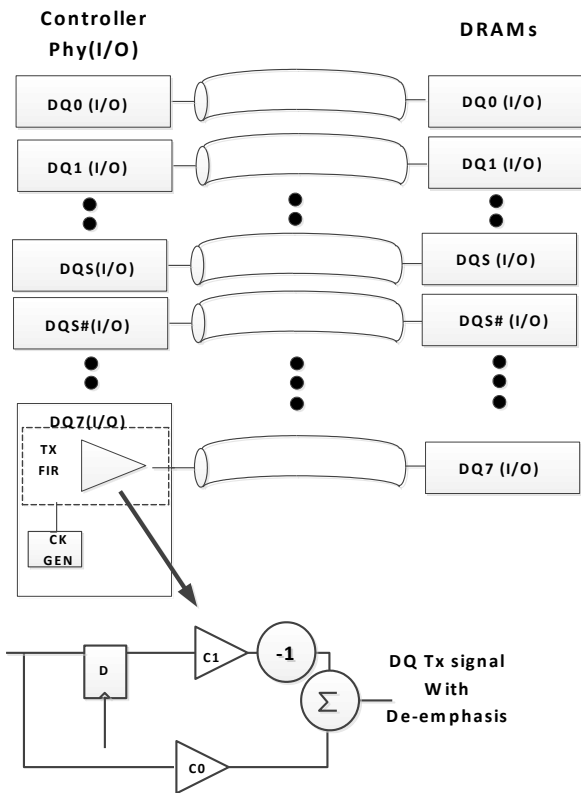# Upper and Lower Routing Eye Diagram Comparison
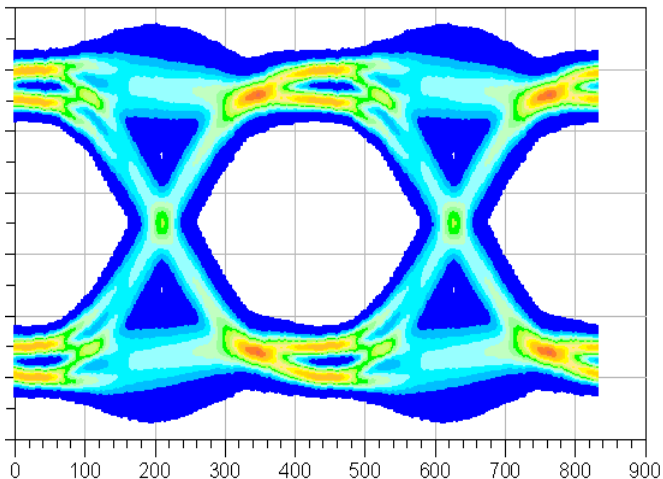
Lower Layer

Upper Layer

~ 7.2% jitter improvement using upper layer

Tx De-emphasis Architecture

$$\sum_{k=0}^{k=1} |ck| = 1$$

$$2\ tap\ De\text{-}emphasis\ Spec(dB) = -20\ log(\frac{Vshelf}{Vswing})$$

$$= -20\ log(\frac{(|c_0|-|c_1|)/2}{(|c_0|+|c_1|)/2})$$

Write Data Eye Improvement with De-emphasis
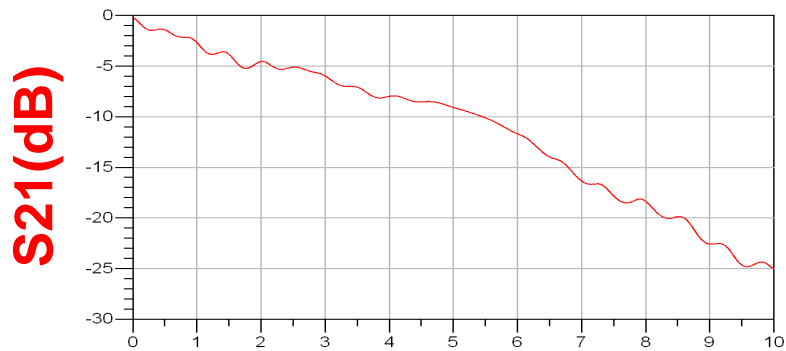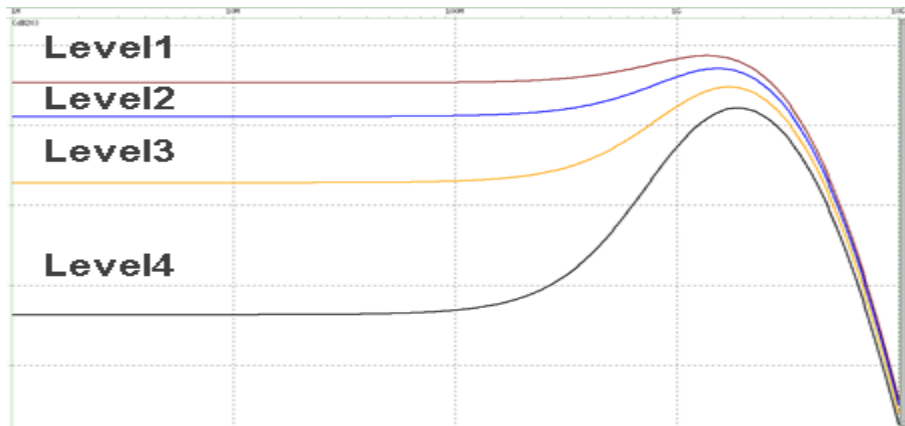

➔ *With De-emphasis ~ 4% improvement*
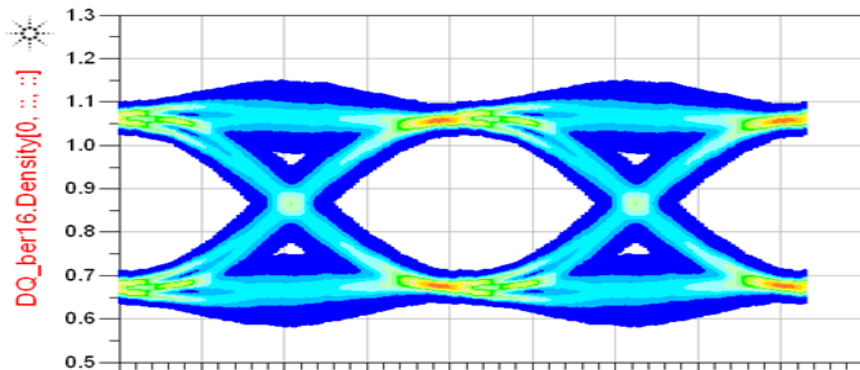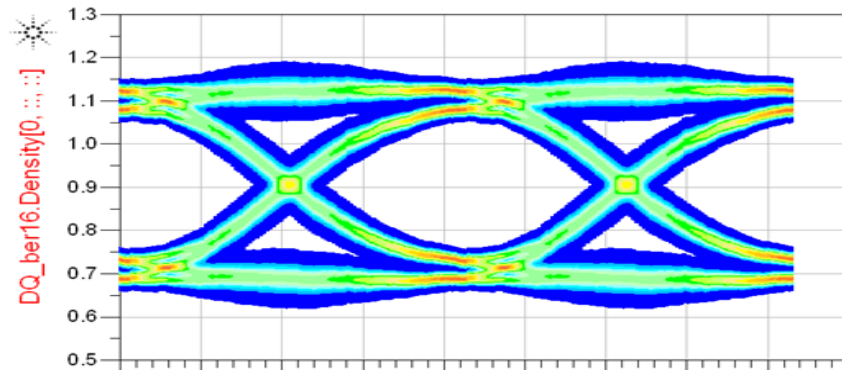
Receiver Continuous Time Linear Equalizer
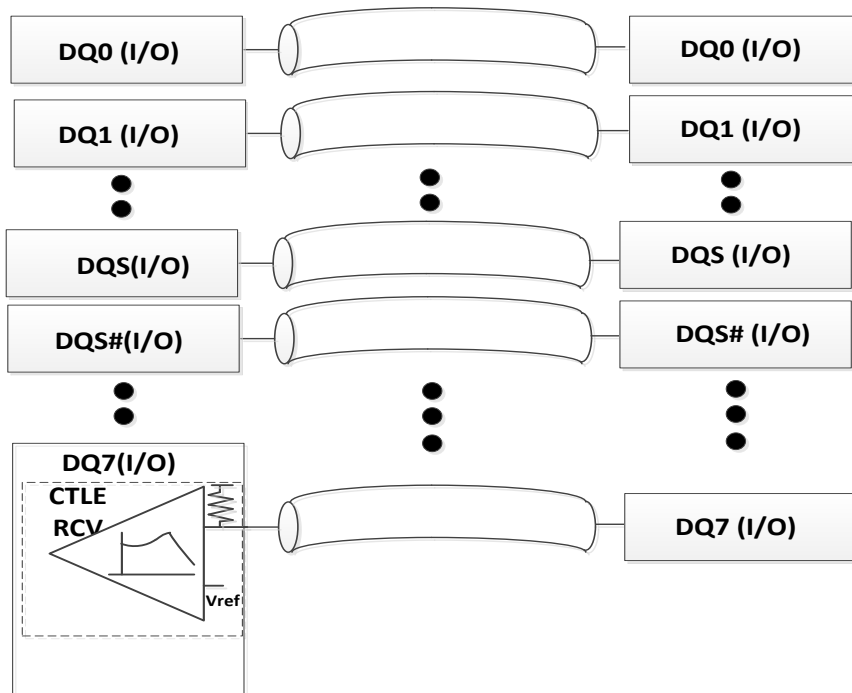
Read Data Eye Improvement with CTLE Improvement
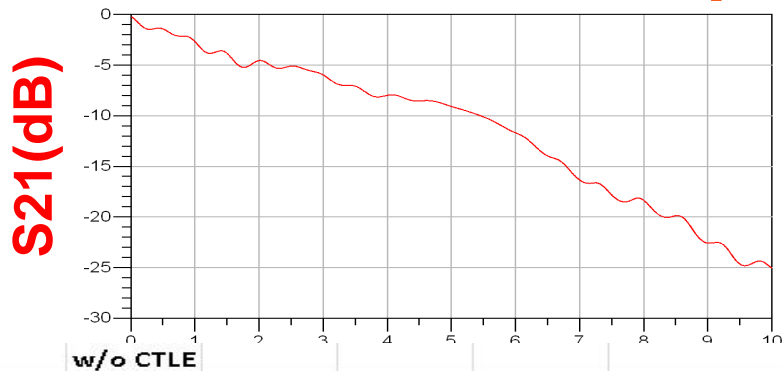
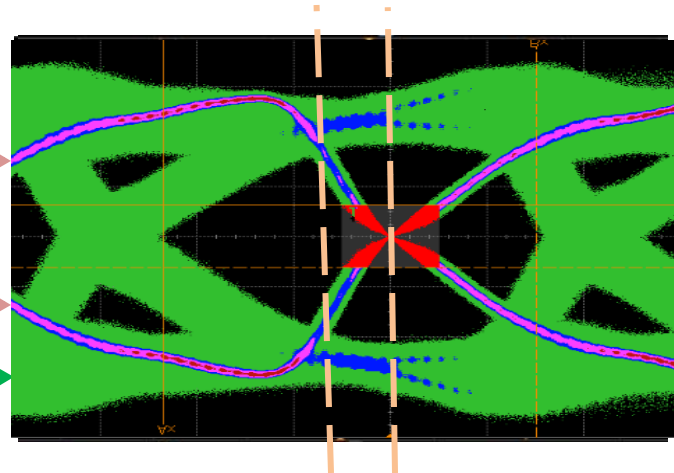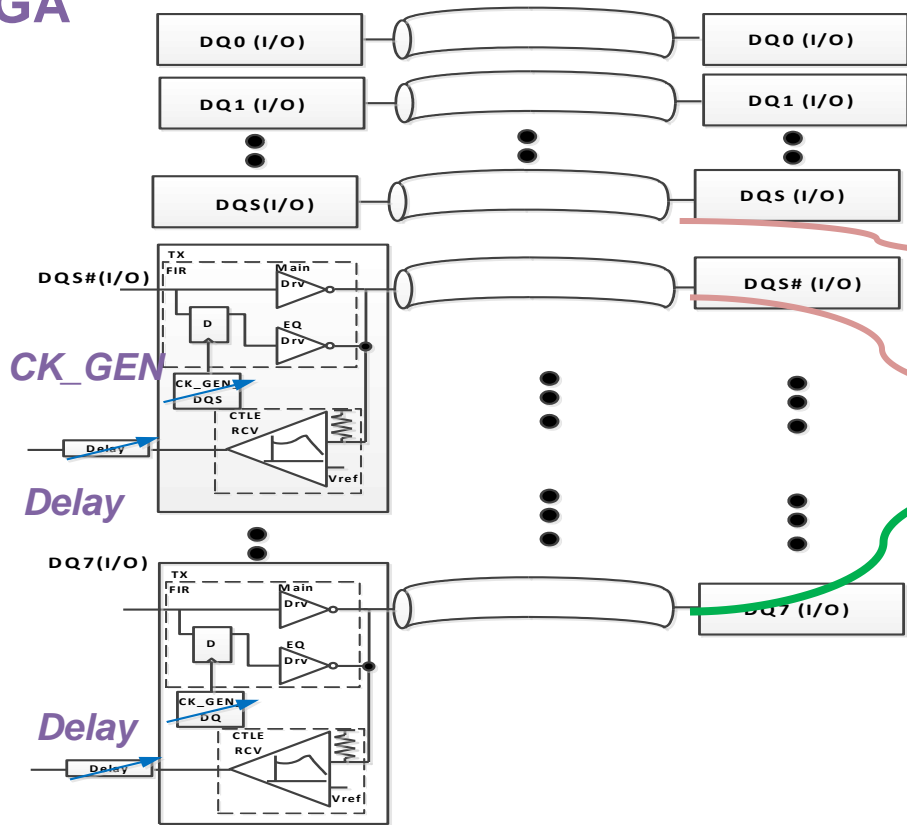→ *With CTLE ~ 12% improvement*
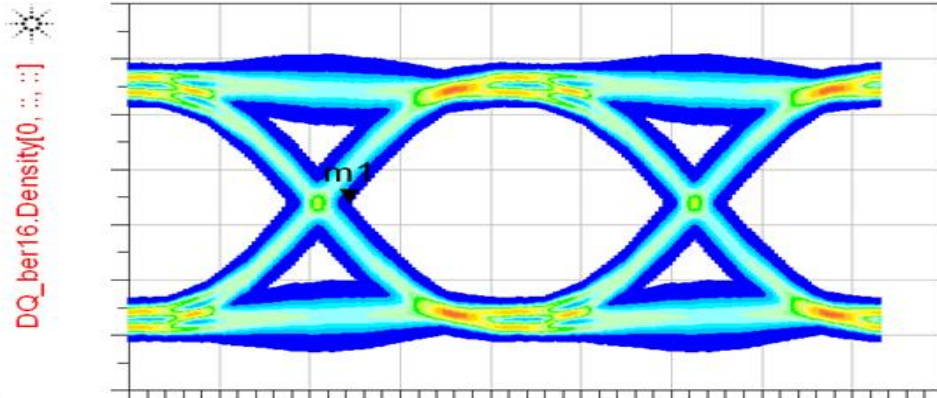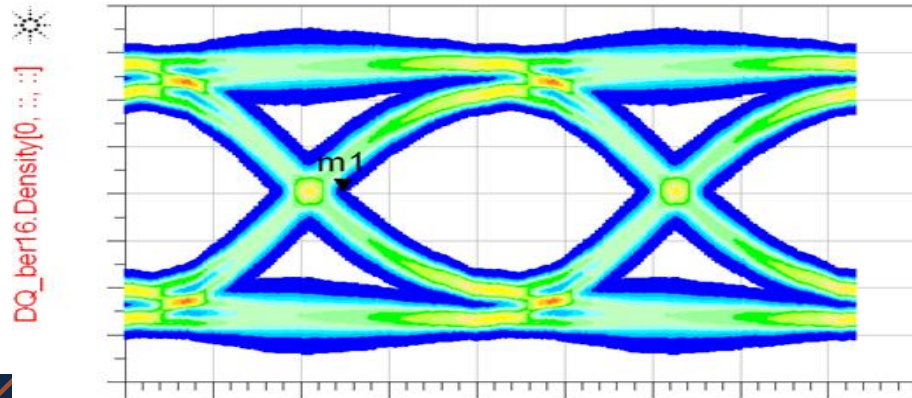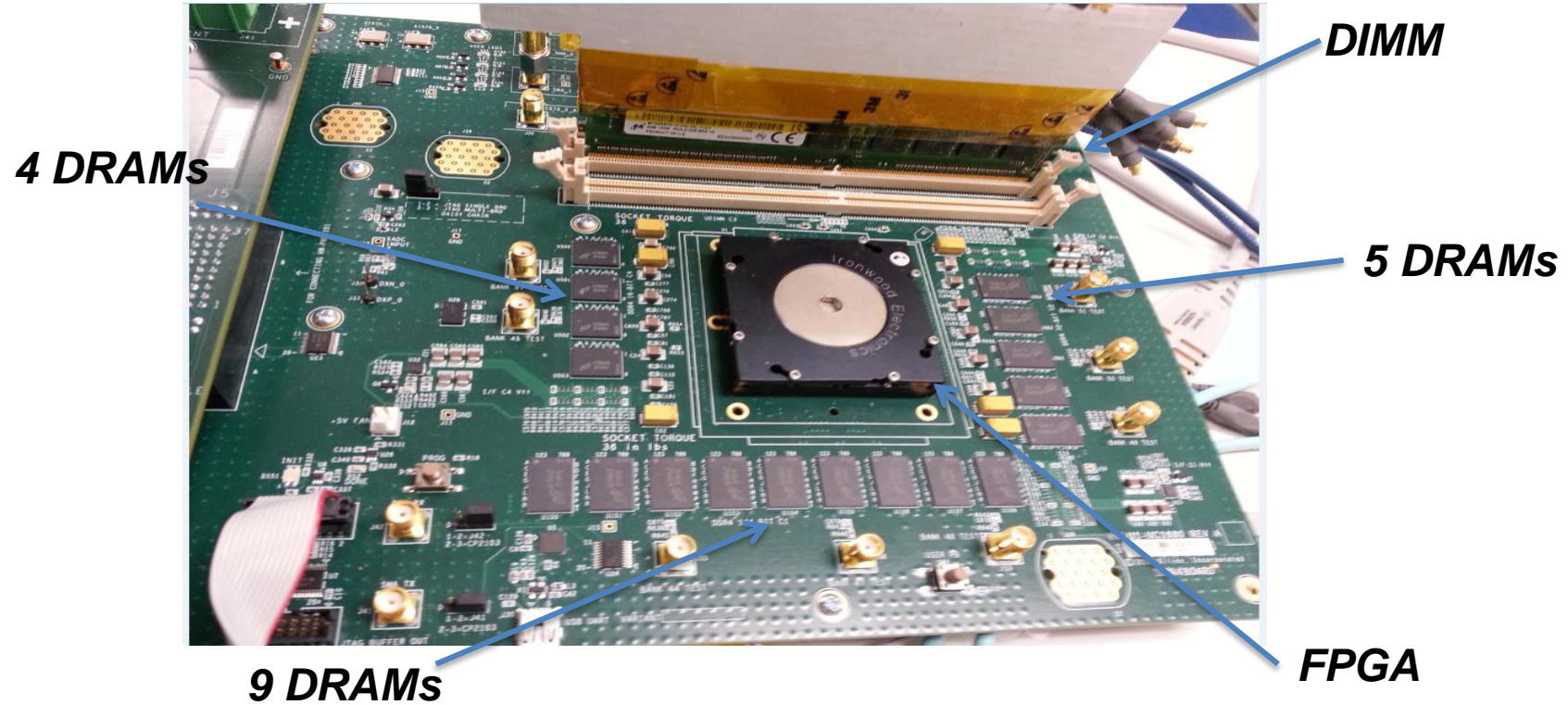
Per Bit De skew Capability

Experimental Data Validation

> **Validation System Configuration**

> **Write Shmoo Procedure Overview**

> **Read Shmoo Procedure Overview**

> **Data Eye Scope Capture**
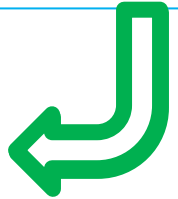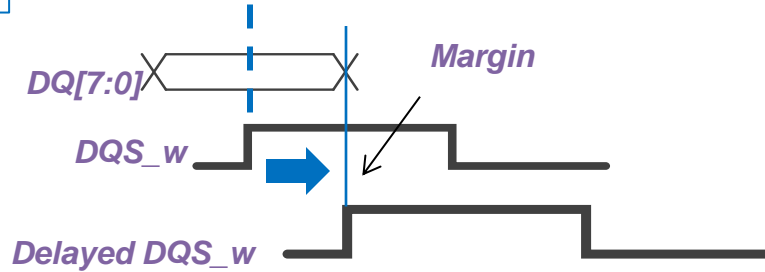
> **Over Clocking Results**
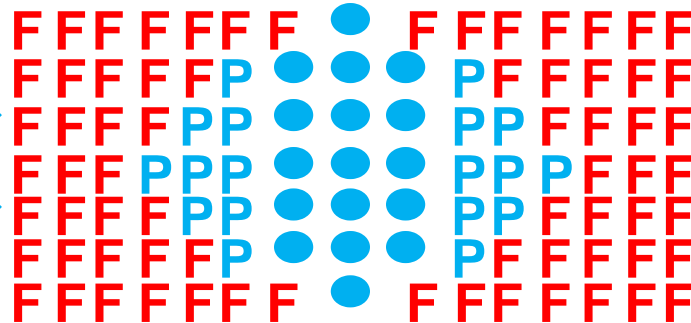
Validation System

Write Shmoo Margining Test Flow

Read Shmoo Margining Test Flow
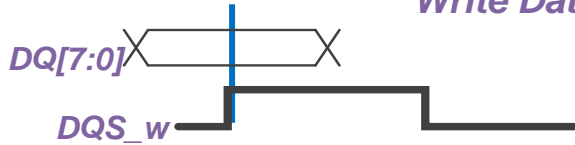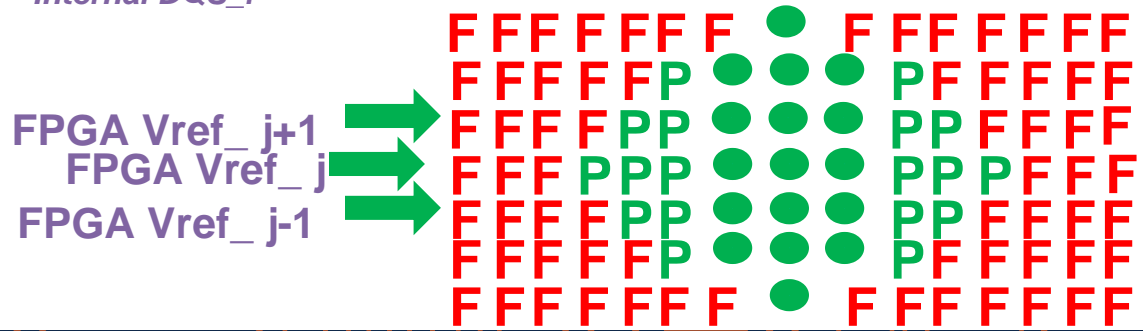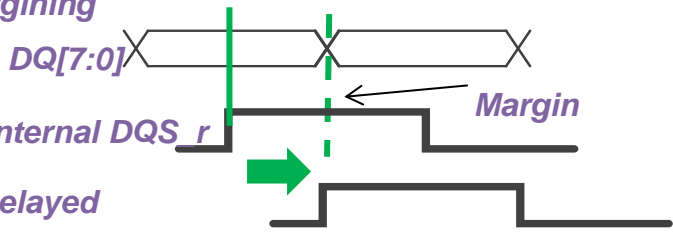
Write and Read Eye Shmoo at 2400MTs
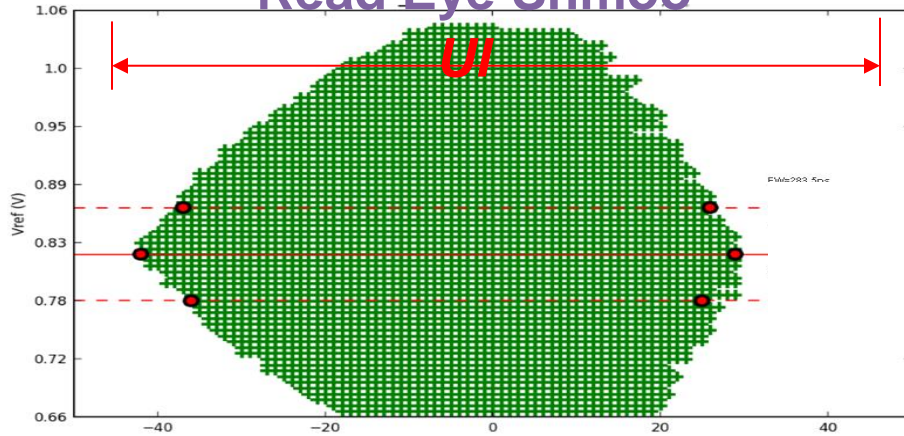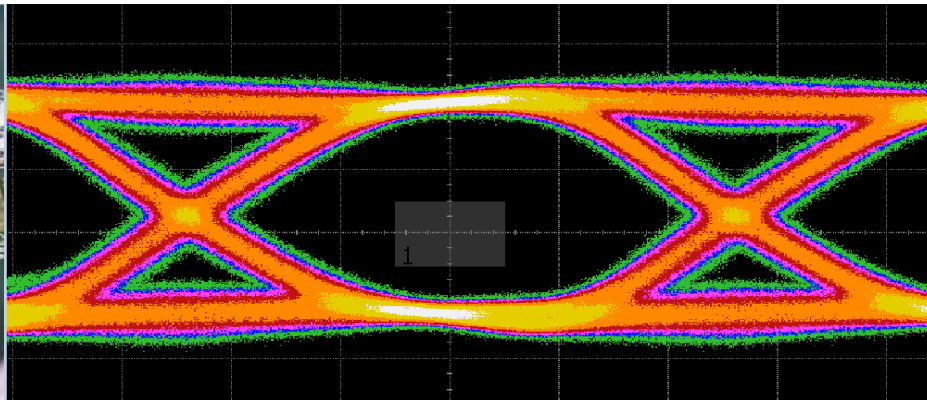

Write Eye Shmoo
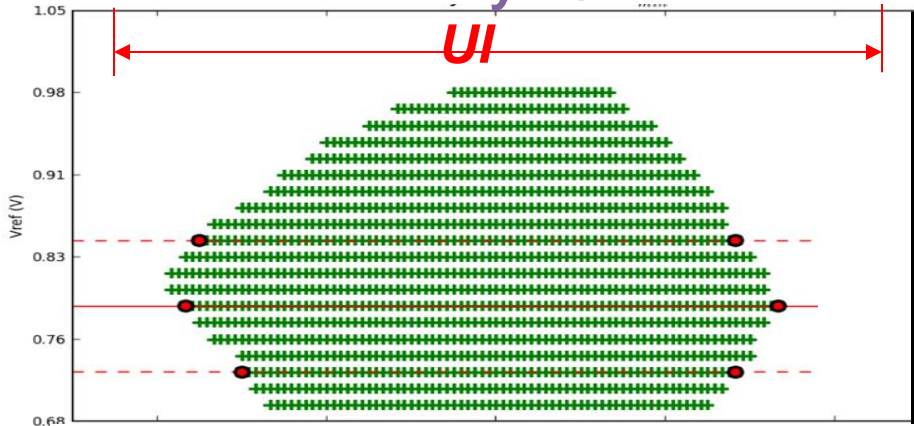
Read Eye Shmoo

DDR4 Memory Write Eye (Scope) Measurement
Write Eye Capture at 2400MTs

Probes Attachment
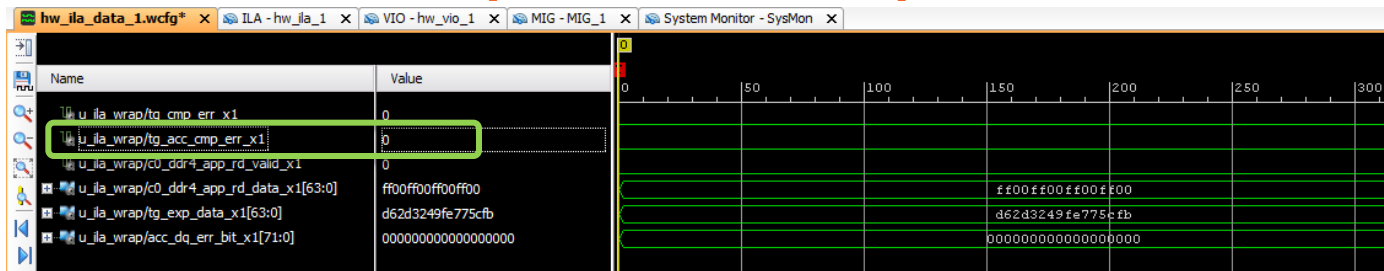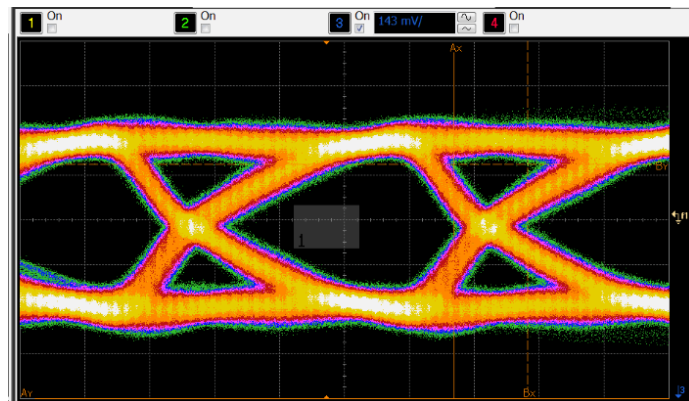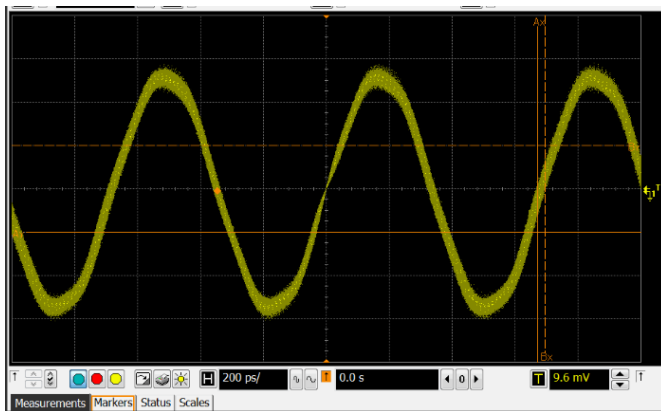
Write Data Eye Capture

Over Clocking Results
(at 2993MTs)

No Error

System Clock has low Jitter.

Data Eye has sufficient margin.

Summary & Conclusions

➤ **A top down systematic approach (including PHY/IO /board/package) using statistical DOE enabled an effective method to ensure design robustness.**

➤ **Besides meeting the design spec., each design factors impacts can be quantified and help making better judgments and trade offs.**

➤ **System enablers such as routing selection, IO equalization circuits improvement were quantified.**

➤ **Validation procedures were overviewed and empirical data showed healthy margin for the DDR4 running at 2400MTs.**

➤ **Over clocking data indicated that the stand alone interface is functioning at 2993MTs with low system clock jitter and sufficient data eye margin.**