An Implementer’s Guide to Low-Power and High-Performance Memory Solutions

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Ming Li, Rambus Inc.
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Memory Interfaces are Important ... Everywhere

AMD Radeon R7950 Black Edition
384-bit bus, 264GB/s, 12 DRAMs
source: anandtech.com

2x32 LPDDR2 ~ 6.4GB/s

AMD & Intel Quad-Channel:
4x64 DDR3 ~ 51.2GB/s/CPU
(hundreds of DRAMs)
Memory Interfaces are Important ... Everywhere

AMD Radeon R7950 Black Edition
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source: anandtech.com
Diversity in Memory Systems

Different system considerations...

- Cost: # devices, packaging, interconnect, assembly
- Performance: Bandwidth, latency, working sets/locality
- Capacity: Min/max, configurability, upgradability
- Power: Thermal limits, energy cost, battery life

... lead to different device & system solutions

- Topologies: Point-to-Point, Multi-Rank, Buffered
- Assemblies: Module, Solder-down, SiP, PoP
- Interfaces: GDDR, DDR, LPDDR, XDR, HMC
Memory BW Requirement Is Growing Rapidly

SmartPhone Example

Dimensioning Use Case:

3D video streaming playback to external display via wireless (WiFi or DLNA) + on-line 3D gaming local

Includes: video, graphics and display sub-systems

Similar trends in CPU/GPU
  – Exacerbated by many-core trend
Memory Interface Needs to Continue Improving

• Conventional interface pin-count is not growing as fast
  – Package-on-Package (PoP) staying at 2x32 DQ bus in near future
    • Combination of PoP ball pitch, DRAM bond pads, package routing
  – High-end GPUs slowly increasing from 256→384→512 bit
  – Servers have slowly migrated to 4×64 bit channels
    → BW/pin must increase to keep up with BW demand

• Virtually all spaces have reached critical power limit
  – Thermal dissipation, battery life, energy cost, or combination
  – Energy/bit must be reduced to achieve higher BW
  – Complicated by BW/pin increase
3D Integration: Potentially Disruptive Technology

• Break the BW/power tradeoff with advanced packaging (e.g. Wide IO)
  – What are challenges for memory interfaces?
  – When and where will 3D integration take off?

• Compare Solutions, not Technologies
  – Solutions will vary across diversity of platforms
  – Conventionally packaged solutions are entrenched, evolving
  – Ultimately, a complex economic decision:
    • Overall cost/benefit, reuse across applications, migration path, ...
Tutorial Goal

• Provide an overview of today’s solution space and why the standards have evolved the way they have with an emphasis on interface *signaling* and *clocking*

• Focus on *3D packaging* as a promising avenue to continue achieving necessary BW and Power
  – Understand the opportunities and key challenges/barriers that exist

• Discuss the role of *signal integrity analysis* in choosing your next solution

• Summarize implementer choices
Outline of Tutorial

• DRAM review [John]
• Conventionally packaged interfaces [John]
  – Evolution of standard interfaces
  – Signaling and clocking at peak bandwidth
  – Bandwidth variation
• 3D Packaging for Memory Applications [Ming]
  – Traditional 3D Packaging Technologies
  – New TSV Based 3D Packaging Technologies
• Signal and power Integrity [Wendem]
  – Signal and power integrity challenges
  – Memory interface analysis methodology
  – Main features of memory interfaces
  – Comparison of emerging standards-based solutions
• Conclusion and Final Comparison [John]
Commodity DRAM Architecture


- DRAM core is RC limited
  - ~50ns row cycle, 5ns column cycle
  - $P = CV^2f$, wires not getting any shorter, V scaling slowly
Challenges in Increasing DRAM Core Bandwidth

• A few general approaches:
  – Finer array segmentation → GDDR ~40% more area than DDR
  – Interleaving bank accesses → access restrictions
  – More parallel data on each cycle → Worse granularity

• Core design may impact efficiency as much as I/O
  – Maintain balance, can’t focus on one item in isolation
  – Even more tradeoffs at system design level
Challenges to Decreasing DRAM Core Power

- Cell capacitance nearly constant with generation to keep refresh times unchanged
- Optimal die size for yield and to drive $/bit down is ~fixed
  - Wire lengths also ~fixed with no minor improvements in fF/μm
  - Increase in banks can help this at higher $
- Process constraints (cheap, low leakage) dictate higher voltages than logic processes, where V scaling has slowed
- Core/IO power split ~65%/35%
- LPDDR4 note:
  - Core reorganized to reduce power
  - Single x32 transitions to 2 x16

(Source: Micron, Mobile Forum 2013)
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Industry Roadmaps – BW and power efficiency

Power efficiency estimates include DRAM IO and core
Today’s two mainstream memory system topologies and types

- **DDR**
  - High capacity (modules) or cost sensitive
  - Mainstream DRAM process
  - General and broad application space

- **LPDDR**
  - Low capacity PoP or short reach direct attach
  - Lower leakage process
  - Battery life and stringent TDP
  - Aggressive power states, self-refresh, and transition times

*Market/topologies lead to different tradeoffs and decisions*
### Key architecture differences - DDR vs. LPDDR

<table>
<thead>
<tr>
<th></th>
<th>DDR</th>
<th>LPDDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device widths</td>
<td>x4, x8, x16</td>
<td>x32, dual x16</td>
</tr>
<tr>
<td>Ranks per channel</td>
<td>Up to 4</td>
<td>Up to 2</td>
</tr>
<tr>
<td>Channel width</td>
<td>Up to x72</td>
<td>x32</td>
</tr>
<tr>
<td>Command/Addressing</td>
<td>Explicit single cycle, high pin count</td>
<td>Encoded multi-cycle, low pin count</td>
</tr>
<tr>
<td>Training</td>
<td>ZQ, DQ W leveling and R/W eye, VREF, read gate, CA training</td>
<td>~same + periodic read gate training</td>
</tr>
<tr>
<td>Prefetch</td>
<td>8-bits (with bank grouping in DDR4)</td>
<td>8-bits</td>
</tr>
<tr>
<td>Die Floorplan</td>
<td>Die pads in center</td>
<td>Die pads on edge</td>
</tr>
<tr>
<td>Power Modes</td>
<td>Base</td>
<td>+ Deep Power Down and Clock Stop</td>
</tr>
<tr>
<td>Refresh modes</td>
<td>Base</td>
<td>+ Temp-comp. refresh and Partial Array Self Refresh</td>
</tr>
<tr>
<td>RAS features</td>
<td>CRC and CA parity</td>
<td>None</td>
</tr>
</tbody>
</table>
Multiple generations of memory technology

- Generations overlap and controller PHYs tend to be backwards compatible
- Memory interfaces are DC-coupled and, thus far, require agreement on the VDDQ voltage
  - Driven by technology shrinkage and power reduction requirements
  - E.g. DDR3 has three variations (base + DDR3L, DDR3U)
- Densities increase requiring more address pins
- Speeds increase requiring interface feature changes as well as changes in the “prefetch” to accommodate the fixed core speed
- DDR has gone through 5 generations over ~20 years
  - DDR4 specification released in 2012
- LPDDR will have gone through 4 generations ~8 years!
  - LPDDR4 specification expected to be publically released this year
## Evolution of DDR

### Key implementer choices to consider
- System configuration and topology
- Data rate and power envelope required
- VDDQ voltage
- Cost and availability through product life cycle
- Available CPHY IP or internal design – complexity (SSTL/PODL)

<table>
<thead>
<tr>
<th>Variables</th>
<th>SDRAM</th>
<th>DDR1</th>
<th>DDR2</th>
<th>DDR3</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD/VDDQ/VDP</td>
<td>3.3/2/5</td>
<td>2.5</td>
<td>1.8</td>
<td>1.5/1.5/-</td>
<td>1.2/1.2/2.5</td>
</tr>
<tr>
<td>Data Rate (Mbps)</td>
<td>166</td>
<td>400</td>
<td>800</td>
<td>1600</td>
<td>3200</td>
</tr>
<tr>
<td>Clock</td>
<td>Single ended</td>
<td>Differential</td>
<td>Differential</td>
<td>Differential</td>
<td>Differential</td>
</tr>
<tr>
<td>Strobes</td>
<td>unsupported</td>
<td>Single ended</td>
<td>Single ended or Differential</td>
<td>Differential</td>
<td>Differential</td>
</tr>
<tr>
<td>Vref</td>
<td>N/A</td>
<td>External</td>
<td>External</td>
<td>Ex/Internal</td>
<td>Ex/Internal*</td>
</tr>
<tr>
<td>ODT</td>
<td>unsupported</td>
<td>unsupported</td>
<td>supported</td>
<td>supported</td>
<td>supported</td>
</tr>
<tr>
<td>Interface</td>
<td>LVTTL</td>
<td>SSTL</td>
<td>SSTL</td>
<td>SSTL</td>
<td>PODL</td>
</tr>
</tbody>
</table>
Evolution of LPDDR

- Key implementer choices to consider
  - System configuration and topology, data rate and power envelope required
    - Unterminated (HSUL) vs. Terminated (PODL/LVSTL)
  - VDDQ voltage
  - Cost and availability through product life cycle
  - Available CPHY IP or internal design - complexity

<table>
<thead>
<tr>
<th>Variables</th>
<th>LPDDR1</th>
<th>LDDR2</th>
<th>LDDR3</th>
<th>LDDR4†</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD1, VDD2, VDDQ (V)</td>
<td>1.8</td>
<td>1.8/1.2/1.2/1.2</td>
<td>1.8/1.2/1.2</td>
<td>1.8/1.1/1.1</td>
</tr>
<tr>
<td>Data Rate (Mbps)</td>
<td>400</td>
<td>1066</td>
<td>2133</td>
<td>4266</td>
</tr>
<tr>
<td>CA</td>
<td>SDR</td>
<td>DDR</td>
<td>DDR</td>
<td>SDR</td>
</tr>
<tr>
<td>Clock</td>
<td>Single ended</td>
<td>Differential</td>
<td>Differential</td>
<td>Differential</td>
</tr>
<tr>
<td>Strobes</td>
<td>Single ended</td>
<td>Differential</td>
<td>Differential</td>
<td>Differential</td>
</tr>
<tr>
<td>Vref</td>
<td>External</td>
<td>External</td>
<td>External</td>
<td>Ex/Internal</td>
</tr>
<tr>
<td>ODT</td>
<td>unsupported</td>
<td>Unsupported</td>
<td>supported</td>
<td>supported</td>
</tr>
<tr>
<td>Interface</td>
<td>SSTL</td>
<td>HSUL</td>
<td>HSUL/PODL</td>
<td>LVSTL</td>
</tr>
</tbody>
</table>

†Based on available public information
Common features for BW/power efficiency improvements

- **Silicon level (CPHY, DRAM)**
  - Improved processes and voltage scaling (but severe slow-down)
  - Improved termination and signaling choices
  - Low jitter clocking techniques
  - Controller PHY complexity – asymmetric system
  - Calibration and eye training (power-up and periodic)
  - Coding - DBI
  - Noise management (SSO, Vref, crosstalk, reference planes)
  - RAS features: Parity and CRC

- **System Level (channel, topology)**
  - Improved package for reducing inductance (L di/dt) and reducing crosstalk
  - Board & connector or co-packaging improvements
  - Reduction of supported ranks; move to point-to-point
Outline of Tutorial

• DRAM review [John]
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  – Evolution of standard interfaces
  – **Signaling and clocking at peak bandwidth**
  – Bandwidth variation
• 3D Packaging for Memory Applications [Ming]
  – Traditional 3D Packaging Technologies
  – New TSV Based 3D Packaging Technologies
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  – Signal and power integrity challenges
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• Conclusion and Final Comparison [John]
Importance of **Signaling** and **Clocking** - Power

- 16 Gb/s graphics memory interface prototype
  - **CTRL**: 65nm G+ ASIC process  **DRAM**: “emulated” 40nm DRAM process
  - Write: 5-tap TX-FIR with CML type driver
  - Read: Continuous time linear equalizer

Lee, et.al. JSSC’08
High-Speed Signaling

- Must treat channels as transmission lines
  - Typically terminated to reduce reflections
  - Impedance discontinuities lead to reflections
    (C_i, vias, connectors, trace/termination impedance tolerances, ...)
  - Dielectric loss and skin-effect lead to pulse dispersion
  - Crosstalk from neighboring pins and traces

- Most memory channels are bi-directional

- Channel equalization approaches:
  - Linear equalizer, transmit FIR, decision feedback equalizer (DFE)
  - Well known in SerDes, just starting to reach high-volume DRAM
    - K. Koo, et al, ISSCC 2012, Paper 2.2 (Hynix DDR4) shows TX pre-emphasis
Differential vs. Single Ended Signaling

Series TX Termination Examples:

- $V_{txd} = I_{txd} \times 2Z_0$
- $V_{rxd} = V_{txd}$

$V_{rxs} = V_{txs} - V_{ref}$

<table>
<thead>
<tr>
<th>Issue</th>
<th>Diff</th>
<th>SE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signaling current:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Differential can achieve $2 \times$ the swing with the same line current</td>
<td>✔</td>
<td></td>
</tr>
<tr>
<td>Robustness (Performance):</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- SE requires reference voltage, more sensitive to noise &amp; crosstalk</td>
<td>✔</td>
<td></td>
</tr>
<tr>
<td>Pin efficiency:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Differential requires twice as many signal pins, or twice the baud rate</td>
<td></td>
<td>✔</td>
</tr>
<tr>
<td>- Caveat: SE typically needs more VDD/VSS pins for supply bounce</td>
<td>✔</td>
<td></td>
</tr>
</tbody>
</table>

- Most SerDes, Intel/AMD parallel busses are differential
- Most high volume DRAMs are single ended
Reducing Driver & Termination Power

- Lower $V_{DDQ}$ ($P \propto V_{DDQ}^2$) or swing ($P \propto V_{swing}$)
  - Transistor headroom limitations, esp. in DRAM process
  - *Sensitive RX is key to reducing swing*
    - Proportional errors such as ISI & crosstalk scale down
    - Fixed errors such as voltage offsets can be calibrated
    - Thermal noise is the ultimate limiter (order of $1mV, \text{rms}$)

- Optimize signaling configuration
  - SSTL (DDR2/3) $\rightarrow$ PODL (DDR4, GDDR3/4/5): lower term. current
  - HSUL in LPDDR removes RX termination entirely
    - CMOS-like signaling, but TX termination still critical
    - Suitable for clean, short (wrt UI) channels and moderate data rates

- Code data (e.g., DBI-AC/DC)
  - Add one bit to a byte and code away from high-power states
Example: Low-swing driver with TX-Regulator

- Low-swing (±100mV, differential)
  - Sensitive RX (offset calibrated)
- Near ground common-mode
  - Can use all NMOS devices
  - Allows simple ESD structure
  \[ I = \frac{V_s}{2 \times Z_d} \]
  \[ \rightarrow \text{Low } Ci \]
- Internal regulator
  - Allows series termination
    (a.k.a. “voltage mode” signaling)
  - Doesn’t require separate \( V_{DDQ} \)

\[ \begin{align*}
  V_{dd} & \quad \text{Regulator} \\
  V_s & \quad I = \frac{V_s}{2 \times Z_d} \\
  Z_d/2 & \quad \text{Vo} = Z_d \times I \\
  Z_d/2 & \quad Z_d/2
\end{align*} \]

*Poulton, et al. JSSC 2007*
Comparison of Signaling Standards

**HSUL**
- Large voltage swings
- Power reduction in most cases
- Limited channels/data rates
- Lower Rx Ci

**SSTL**
- VREF at VDDQ/2
- Much improved SI over HSUL allowing expansion of channels/data rates

**PODL**
- Lower termination/DC power - high logic level has I=0
- DBI can be used
- VREF AC coupled to a single supply

**LVSTL**
- Lower termination/DC power - low logic level has I=0
- DBI can be used
- VREF AC coupled to lowest Z supply
- VDDQ agreement may not be req’d
- N over N driver -> Ci reduction and allows aggressive VDDQ scaling
Signaling Standards – Swing, VREF, and Current

**HSUL:**
Swing = VDDQ
IH = 0
IL = 0
(Only dynamic switching power)
VREF = VDDQ/2

**SSTL:**
Swing = 2RT/(RS+RT)*VDDQ/2
IH = VDDQ / 2(RS+RT)
IL = VDDQ / 2(RS+RT)
VREF = VDDQ/2

**PODL:**
Swing = RT/(RS+RT)*VDDQ
IH = 0
IL = VDDQ / (RS+RT)
VREF = ((2RS+RT)/(RS+RT))*VDDQ/2

**LVSTL:**
Swing = RT/(RS+RT)*VDDQ
IH = VDDQ / (RT+RS)
IL = 0
VREF = RT/(RS+RT)*VDDQ/2
HSUL & PODL I/O Power Comparison

Notes:
- Weaker PODL termination reduces DC power, but increases switching power
- At 2X data-rate, switching power doubles, but DC power remains constant
- Assumption: 4.7pF total capacitance, 1.2V VDD
- DBI AC can reduce switching power
- DBI DC can reduce termination power
Termination Values (RS and RT)

• Memory system channel impedances
  – Tend to be near 50ohm standard adopted by test equipment and high-speed serial links
  – Package impedances tend to be lower than 50ohms
  – Lower impedances lead to higher bandwidth \((Z_0C_i\) product)

• Matched termination values
  – Best signal integrity
  – Higher power than the alternative

• Under-terminated values
  – Higher voltage swings (low RS, high RT)
  – Lower power (high RT)
  – Increased reflections and more management of SI
System Level Clocking

- System timing synchronous to CK generated by CPHY
  - Used directly for CA bus which is uni-directional
  - Source of internal DRAM clock (DCLK)
- Read/writes use a bi-directional, differential strobe (RDQS/WDQS)
  - Improved source jitter tracking
- Both CK and strobes run at half the DQ transfer rate (DDR)
- Many critical timing paths to consider that could limit performance
- More timing domains introduced as BW increases
  - DDR data clock (1.6GHz for 3.2Gbps) higher than most ASIC internal clocks
Generic xDDR Direct Strobe System – Clocking & Critical Timing Paths

Controller IO

- **RDATA RDBI**
- **WDATA WDBI**
- **WDQS**

Channel

- **DQ**
- **DRAM IO**

- **Omux**
- **Pre**

- **Drive**
- **Isamp**

- **ReTime**

- **Ref**

- **CA**
- **Cmd Address**
- **PCLK**

- **WDQS/RDQS/#[10:9]**
- **WDQA/RE[7:0]**
- **WDBI/RDBI[8]**

1) tRdqsPclk 2) tRdqRdqs 3) tWdqWdqs 4) tWdqsDclk 5) tCaDclk 6) tCK

**System Level Clocking (cont.)**
RDQS to CK uncertainty

- DDR: uses a DLL on DRAM to phase align the Read strobe, RDQS, and data, RDQ, with incoming CK
- LPDDR: foregoes the DLL to reduce power and DRAM wakeup time
  - Increased variability of read data return with respect to fixed read latency (tDQSCK)
  - Requires tracking and gating of the strobe signal by the CPHY to accommodate increased drift
  - Net: increased controller complexity and another system level timing budget item
Why is a DLL used in DRAM?

Compensates static and dynamic timing error between CK and WDQS.
Internal Clock Generation and Distribution

• Every data bit needs to be clocked, often more than once
  – Amortize clock gen. across links, but still need to distribute
  – Clock has 100% activity factor
• Double-edge clocking
  – Efficient: clock frequency = ½ data rate
  – Practical: easier to trim than multi-phase clocks (just DCC)
• CMOS or CML Clocking?
  – CMOS: often preferred at moderate rates
    • Simple, works with CMOS gates and sense-amplifiers 😊
    • Supply-induced jitter (PSIJ) is bad, not improving with process scaling 😞
  – CML: << supply sensitivity 😊 → common at very high speeds
    • Active power not as bad as its reputation (similar to CMOS 😊)
    • Frequency scalability, clock gating are more challenging 😞
    • CML-compatible TX/RX front-end (or convert to CMOS) 😞

  – Configurable for flexibility:  
    K. Sohn et al, ISSCC 2012 Paper 2.1 (Samsung DDR4 DLL)
### Standards Comparison Summary – Signaling & Clocking

<table>
<thead>
<tr>
<th></th>
<th>Signaling</th>
<th>VDDQ</th>
<th>RS</th>
<th>RT†</th>
<th>Clocking</th>
<th>Additional Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR3</td>
<td>SSTL</td>
<td>1.5, 1.35, 1.25</td>
<td>34, 40, 48</td>
<td>20, 30, 40, 60, 120</td>
<td>DLL; SDR CA; DQ + CA eye training</td>
<td></td>
</tr>
<tr>
<td>DDR4</td>
<td>PODL</td>
<td>1.2, 1.05</td>
<td>34, 40, 48</td>
<td>34, 40, 48, 60, 80, 120, 240</td>
<td>DLL; SDR CA; DQ + CA eye training</td>
<td></td>
</tr>
<tr>
<td>LPDDR2</td>
<td>HSUL</td>
<td>1.2</td>
<td>NA</td>
<td>NA</td>
<td>No DLL; DDR CA; DQ eye training</td>
<td></td>
</tr>
<tr>
<td>LPDDR3</td>
<td>HSUL/PODL</td>
<td>1.2</td>
<td>NA/34, 40, 48</td>
<td>NA/120, 240</td>
<td>No DLL; DDR CA; DQ + CA eye training</td>
<td>Termination required for speeds &gt; ~1600Gbps</td>
</tr>
<tr>
<td>LPDDR4</td>
<td>LVSTL</td>
<td>1.05-1.2?</td>
<td>?</td>
<td>?</td>
<td>No DLL; SDR CA; DQ + CA eye training</td>
<td>Based on public statements</td>
</tr>
</tbody>
</table>

†Multi-rank systems tend to split RT termination
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  – Evolution of standard interfaces
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• 3D Packaging for Memory Applications [Ming]
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  – New TSV Based 3D Packaging Technologies
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  – Signal and power integrity challenges
  – Memory interface analysis methodology
  – Main features of memory interfaces
  – Comparison of emerging standards-based solutions
• Conclusion and Final Comparison [John]
• Average efficiency often worse than peak efficiency
  – And more important!
• Utilization *varies with time*
  – Need to consider dynamics

*Luiz Barroso & Urs Hölzle, IEEE Computer, December 2007*
Efficiently Dealing with BW Dynamics

- May trade peak efficiency for average efficiency
  - Avoid efficient but fixed constant power techniques

Memory Interface Properties:
- Net bandwidth varies by orders of magnitude
- Time scales also vary by orders of magnitude:
  - Application launch / state change (~100 millisecond)
  - User response (~10 millisecond)
  - CPU context switch (~microsecond)
  - Random cache miss (~10 nanosecond)
- What is best approach to variable bandwidth?
Dynamic Bandwidth & Power Scaling

- **Variable Bit-Rate (DVFS)**†
  - Better than proportional power scaling
    - But slow response for VDD scaling, reconfiguration
    - Frequency scaling alone hurts efficiency
  - Complicated design & test, limited range (e.g., 3-5×)
  - Alt: Scaling # of active links has some similar challenges

- **Burst Transactions at Peak Rate**
  - Suited to very fast, wide dynamic shifts
  - Optimize link at one data rate
  - Common in current mobile memory systems
  - Key metric: wakeup time vs. burst length

†G. Balamurugan, et al., JSSCC, April 2008 is a good example
Dynamic BW Memory Systems

- Support for burst-mode (clock stop mode) present in LPDDR
- All memory systems implicitly support frequency scaling (both half-rates and non-integer frequency hopping)
  - Only big difference is the transition time supported by the DRAM and the controller
- So far, no DVFS
  - Scaling of IO voltages on DRAM would be significant change
Burst Mode Challenges in High Speed Links

CPU Memory

PLL/DLL:
- Typically slow startup
- Eliminate, at least on DRAM

Resonant Clocking:
- Can’t synchronously gate resonant node
- Complex downstream clock gating

Analog Circuits:
- Minimize Use
- Fast startup when needed (TX regulator, CML, etc.)
Example: 4.3 GB/s Mobile Memory Interface w/ Power Efficient BW Scaling

Conventionally Packaged Interface Summary

- Bandwidth and efficiency must continue to improve
  - Average or effective power more relevant than peak power

- Active research area for conventionally packaged interfaces:
  - Increasing use of equalization & crosstalk cancellation
  - Low-swing signaling with RX offset calibration
  - Remove expensive local delay matching buffers
  - Faster wakeup times with zero idle power
  - DVFS for slower dynamics and “drowsy” modes
Outline of Tutorial

- DRAM review [John]
- Conventionally packaged interfaces [John]
  - Evolution of standard interfaces
  - Signaling and clocking at peak bandwidth
  - Bandwidth variation
- 3D Packaging for Memory Applications [Ming]
  - Traditional 3D Packaging Technologies
  - New TSV Based 3D Packaging Technologies
- Signal and power Integrity [Wendem]
  - Signal and power integrity challenges
  - Memory interface analysis methodology
  - Main features of memory interfaces
  - Comparison of emerging standards-based solutions
- Conclusion and Final Comparison [John]
Traditional 3D Packaging for Memory Application – System-in-Package (SiP)

- System-in-Package (SiP)
  - Die stacking using wire bond (WB) interconnects
  - Same memory die stacking for memory capacity (NAND or DRAM)
  - Logic/memory die stacking for memory bandwidth (BW)
  - Low cost solution
  - Limited BW scalability due to limited WB interconnect density
  - Know-Good-Die (KGD) concern

(Source: Internet)
Traditional 3D Packaging for Memory Application – Package-on-Package (PoP)

- Package-on-Package (PoP)
  - Top memory package
  - Bottom logic package
  - Logic and memory packages separated for logistic control and KGD
  - JEDEC defined standard memory interface between top and bottom
    - Recently more non-standard approaches in Apple and Samsung products
  - Limited BW scalability due to limited interface memory bus width
    - Scaling with memory technology scaling, LPDDR2 -> LPDDR3 -> LPDDR4
  - Mainly for mobile application
    - Dominating in high end smart phones

(Source: Internet)
Memory PKG Trends for Smartphone Application

PoP for middle to high-end, MCP (SiP) for low to middle-end

<table>
<thead>
<tr>
<th>Year</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-end</td>
<td>LPDDR2</td>
<td>LPDDR3</td>
<td>LPDDR3</td>
<td>LPDDR3</td>
</tr>
<tr>
<td>Low-end</td>
<td>LPDDR</td>
<td>LPDDR</td>
<td>LPDDR2</td>
<td>eMCP</td>
</tr>
</tbody>
</table>

MCP = SLC NAND and Mobile DRAM
eMCP = eMMC and Mobile DRAM
POP (Package on Package) = Mobile DRAM

(Minho Kim, Sk hynix, SemiCon West 2013)
PoP Basic Parameters

A – PoP Pkg size, JEDEC defined 12 or 14 mm
B – PoP total height, trends from 1.4 -> 1.2 -> 1.0 mm
C – Interface BGA ball pitch, JEDEC defined 0.5 or 0.4 mm, TMV for smaller pitch
D – Interface BGA ball count, most import parameter for BW scaling
# JEDEC Defined PoP Ball Count vs. Memory BW

<table>
<thead>
<tr>
<th>Pkg Size (mm^2)</th>
<th>Interface BGA Ball Pitch (mm)</th>
<th>Interface Ball Count</th>
<th>Memory BW for 2Ch x32 (GB/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 x 12</td>
<td>0.4</td>
<td>216</td>
<td>6.4 for LPDDR2</td>
</tr>
<tr>
<td>14 x 14</td>
<td>0.4</td>
<td>256</td>
<td>12.8 for LPDDR3</td>
</tr>
<tr>
<td>14 x 14</td>
<td>0.5</td>
<td>240*</td>
<td>6.4 for LPDDR2</td>
</tr>
<tr>
<td>15 x15</td>
<td>0.5</td>
<td>216</td>
<td>12.8 for LPDDR3</td>
</tr>
</tbody>
</table>

* Three interface BGA rows, 3rd row depopulated
JEDEC 12 mm/0.4 mm, 216 Ball PoP for 2CH x32 LPDDR2 Ballout
PoP New Trends: Non-JEDEC Formfactor

iPhone 5S (A7 SoC) – 1GB LPDDR3
14x15.5 mm, 456-Ball, 0.35mm pitch
BW = 12.8 - 17 GB/s

iPhone 5 (A6 SoC) – 1GB LPDDR2
14x15.5 mm, 272-Ball, 0.4mm pitch
BW = 6.4 - 8.5 GB/s

From: Chipworks
Graphics is driving memory BW requirement in mobile systems

(Minho Kim, SK hynix)
Next Generation Mobile DRAM

(Minho Kim, SK hynix)
TSV Based 3D Packaging Technology for Memory Application – Wide IO DRAM

<table>
<thead>
<tr>
<th></th>
<th>WideIO</th>
<th>LPDDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>1.2 volts</td>
<td>1.2 volts</td>
</tr>
<tr>
<td>Speed</td>
<td>200 Mbps</td>
<td>1600 Mbps</td>
</tr>
<tr>
<td>Data width</td>
<td>512 bits</td>
<td>32 or 64 bits</td>
</tr>
<tr>
<td>Data rate</td>
<td>single</td>
<td>double</td>
</tr>
<tr>
<td>Maximum channel bandwidth</td>
<td>12.8 GB/s</td>
<td>@32 bits -- 6.4 GB/s</td>
</tr>
</tbody>
</table>

- **Low power for mobile application**
  - Much better performance/power, power efficiency than LPDDRx
- **Small formfactor**
  - Thin profile and smaller x/y footprint
- **Better thermal performance than LPDDRx PoP**
- **High cost associated with TSV**
- **Complicate business model**
  - Yield loss
  - Scrap management

(Source: Internet)
Wide IO2 vs. LPDDR3/4

(Hung Vuong, Qualcomm, JEDEC Mobile Forum 2013)
Wide IO vs. PoP

WIO2 takes revolutionary path, showing significant difference than LPDDRx

(Minho Kim, Sk hynix, SemiCon West 2013)
TSV Based 3D Packaging Technology for Memory Application – Hybrid Memory Cube (HMC)

Fast process logic and advanced DRAM design in one optimized package

- Power Efficient
- Smaller Footprint
- Increased Bandwidth
- Reduced Latency

(Source: MemCon Memory Conference 2012)
HMC Memory Interface

HMC (Gen2) has Four Links
Each Link has 32 differential Lanes
(*) HMC-SR supports up to 15Gbps SERDES options

Design with Off-the-Shelf, High Speed SerDes Interface

**Link Interface Examples**

- **4 Link Example (160GB/s)**
  - 10Gb/s per lane
  - 32 lanes per link (320Gb/s = 40GB/s)
  - 16 TX and 16 RX
  - 4 Links (40GB/s x 4) = **160GB/s**

(Source: Mike Black, Micron, EDPS 2013)

(*) Aggregate DRAM peak bandwidth remains 160GB/s
HMC Applications

- HMC SR-15 (Gen2) for HPC/Server (CPU) & Network (NPU) Applications
  - Short reach channel with 12 dB of insertion loss
  - 160 GB/s Memory BW
  - 10, 12.5, 15 Gb/s SERDES interface
  - 2/4GB memory density
  - 31 x 31 mm 4-link package
  - 16.5 x 19 mm 2-link package
TSV Based 3D Packaging Technology for Memory Application - High Bandwidth Memory (HBM)

(Source: SK/Hynix, Jan 2013)
HBM Applications

- CPU for HPC applications, GPU for graphic application, and NPU for network application
- 1024 bit bus width, 1 Gb/s signaling (Gen1), DDR memory interface, total 128 GB/s memory BW
- On a Si interposer, need probing on micro-bump
<table>
<thead>
<tr>
<th></th>
<th>HBM</th>
<th>HMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Signaling (Gb/s)</td>
<td>2 (Gen 2)</td>
<td>20 - 30 (Gen 3)</td>
</tr>
<tr>
<td>Bus Width (bit)</td>
<td>1024</td>
<td>4 Links (16 lane per link, bi-directional)</td>
</tr>
<tr>
<td>Max BW (GB/s)</td>
<td>256</td>
<td>320 - 480</td>
</tr>
<tr>
<td>PHY</td>
<td>Memory PHY only</td>
<td>Memory/Controller PHYs in serial links</td>
</tr>
<tr>
<td>Format</td>
<td>In a Si Interposer</td>
<td>Stand alone as a complete package, No KGD issue</td>
</tr>
<tr>
<td>Standardization</td>
<td>JEDEC</td>
<td>HMC Consortium</td>
</tr>
<tr>
<td>Applications</td>
<td>Graphic, HPC, Network</td>
<td>Network, HPC, Server</td>
</tr>
</tbody>
</table>
## HBM vs. Wide IO2

<table>
<thead>
<tr>
<th>ITEM</th>
<th>Mobile WIO2</th>
<th>HBM (High B/W Memory)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bottom die</td>
<td>N/A</td>
<td>Buffering &amp; Signal re-routing</td>
</tr>
<tr>
<td>BW (GB/s)</td>
<td>25.6~51.2</td>
<td>128~256</td>
</tr>
<tr>
<td>Pin Speed</td>
<td>0.4~0.8 Gbps</td>
<td>1~2 Gbps</td>
</tr>
<tr>
<td># I/O</td>
<td>512</td>
<td>1,024</td>
</tr>
<tr>
<td># Bump Logic</td>
<td>1~2K</td>
<td>6K~8K</td>
</tr>
<tr>
<td># Bump DRAM</td>
<td>1~2K</td>
<td>~3K</td>
</tr>
<tr>
<td>Cube (GB)</td>
<td>1 / 2</td>
<td>1 / 2 / 4</td>
</tr>
<tr>
<td># TSV stack</td>
<td>1 / 2 / 4</td>
<td>1 / 2 / 4</td>
</tr>
<tr>
<td>DRAM density</td>
<td>8Gb</td>
<td>8Gb</td>
</tr>
<tr>
<td>Application</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GFX card</td>
<td>o</td>
<td>o</td>
</tr>
<tr>
<td>ULT</td>
<td>o</td>
<td>-</td>
</tr>
<tr>
<td>HPC</td>
<td>-</td>
<td>o</td>
</tr>
<tr>
<td>Server</td>
<td>-</td>
<td>(o)(Cache)</td>
</tr>
<tr>
<td>Mobile</td>
<td>o</td>
<td>-</td>
</tr>
</tbody>
</table>

(Bob Brennan, Samsung, Memcon 2013)
Markets for TSV Based 3D Packaging Technologies

<table>
<thead>
<tr>
<th>Market</th>
<th>SmartPhone</th>
<th>Tablet</th>
<th>Networking</th>
<th>Graphics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor</td>
<td>Apps Processor</td>
<td>Apps Processor</td>
<td>Networking Proc</td>
<td>Graphic Proc</td>
</tr>
<tr>
<td>Power</td>
<td>1-2W</td>
<td>1-5W</td>
<td>20W +</td>
<td>20W +</td>
</tr>
<tr>
<td>Memory Type</td>
<td>Wide I/Ox</td>
<td>Wide I/Ox or LPDDRx</td>
<td>HMC / HBM</td>
<td>HBM</td>
</tr>
<tr>
<td>Memory Size</td>
<td>2 → 4 GB</td>
<td>4 → 8 → 16 GB</td>
<td>4 → 8 → 16 GB</td>
<td>4 → 16 GB</td>
</tr>
<tr>
<td>Interface</td>
<td>Wide I/O2</td>
<td>Wide I/O or DDR</td>
<td>SerDes / Parallel</td>
<td>Parallel</td>
</tr>
<tr>
<td>I/O</td>
<td>1000</td>
<td>1000 or 500</td>
<td>&lt;500 / &gt;1000</td>
<td>1600 +</td>
</tr>
<tr>
<td>Min Bump Pitch</td>
<td>40x40µm rows</td>
<td>40x50µm rows or 80µm rows</td>
<td>1mm / 96x55µm array</td>
<td>96x55µm array, staggered rows</td>
</tr>
<tr>
<td>Packaging</td>
<td>3D</td>
<td>2.5D medium L/S density or 3D with heat management</td>
<td>Off chip memory or 2.5D high density interposers</td>
<td>2.5D high density interposers</td>
</tr>
</tbody>
</table>

(Source: Internet)
I would like to acknowledge the Rambus SSE engineers, especially Will Ng and Dave Secker, for contributions and many helpful discussions over the years.
Outline of Tutorial

• DRAM review [John]
• Conventionally packaged interfaces [John]
  – Evolution of standard interfaces
  – Signaling and clocking at peak bandwidth
  – Bandwidth variation
• 3D Packaging for Memory Applications [Ming]
  – Traditional 3D Packaging Technologies
  – New TSV Based 3D Packaging Technologies
• Signal and power Integrity [Wendem]
  – Signal and power integrity challenges
  – Memory interface analysis methodology
  – Main features of memory interfaces
  – Comparison of emerging standards-based solutions
• Conclusion and Final Comparison [John]
Challenges of Memory Systems

- Memory data rates have doubled every four years for main memory and every two years for mobile memory at a similar or lower power envelope.

- The increased performance and reduced power present very difficult SI/PI challenges:
  - Inter-symbol interference (ISI) and crosstalk
  - Impedance discontinuities (stubs, connector, via, etc.)
  - Power supply noise (simultaneous switching output noise)
  - Power supply noise induced jitter
  - Pin-to-pin skew, clock and data jitter
  - Poor transistor performance

- In-depth SI and PI analyses are essential in the design of these power-efficient memory interfaces.
Traditional SI/PI Analysis

- Electrical specification of memory devices consists of a set of measured electrical parameters
- The parameters are related to timing jitter, input/output voltage levels and reflect worse case performance of the complete system
  - With linear or mean square sum of voltage and timing budget analysis
  - Time domain based simulations under worse case conditions
- At the higher data rates, the traditional direct frequency and time-domain methods are no longer sufficient to design and optimize
  - Decouples voltage noise and timing jitter and leads to over design

Example of:

### Timing Budget

<table>
<thead>
<tr>
<th>Components</th>
<th>WRITE (ps)</th>
<th>READ (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Controller</td>
<td>140</td>
<td>90</td>
</tr>
<tr>
<td>DRAM</td>
<td>140</td>
<td>215</td>
</tr>
<tr>
<td>Channel</td>
<td>300</td>
<td>275</td>
</tr>
<tr>
<td>Others</td>
<td>45</td>
<td>45</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>625</strong></td>
<td><strong>625</strong></td>
</tr>
</tbody>
</table>

### Voltage Budget

<table>
<thead>
<tr>
<th>Components</th>
<th>WRITE (mV)</th>
<th>READ (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX Swing</td>
<td>1000</td>
<td>850</td>
</tr>
<tr>
<td>Receiver Vin</td>
<td>300</td>
<td>150</td>
</tr>
<tr>
<td>Channel</td>
<td>700</td>
<td>700</td>
</tr>
</tbody>
</table>

Each parameter can have deterministic and random components
System-Based Approach

- BER-based method that considers the statistical distributions of both voltage and timing parameters is critical to optimize the link performance
  - to consider the interaction
  - to make trade-off between active circuitries and passive channel
  - to consider other system constraints
  - to predict the effect of the components variations on the performance of the complete system
  - and optimize the system in cost and power
  - to verify that the system meets the targeted low BER.
Forwarded Clocking of Memory Links

- Majority of memory interfaces are source synchronous links
  - The clock and data start from the same device and travel the same path
  - Often the clock is distributed across a byte or two
- The clock skew is adjusted to the center of the data at the receiver
- Noise 1: Common to DQ and DQS, correlated jitter tracked
  - Uncorrelated jitter is not tracked: delay difference and noise frequency
  - Noise 2, Noise 3 and Noise 4: Jitter may not be tracked
- Power supply induced jitter is the main source of timing uncertainty
The PDN impedance peaks -10 MHz – 400 MHz is caused by variations in currents drawn from the PDN.
Supply Rails and PSIJ of Clock Path

- Low-impedance power distribution network
- On-chip decoupling capacitance
- Current profile
- Jitter sensitivity
Power Supply System Architecture

- Supply Partitioning to control noise and its impacts
  - Identify circuits generating (large) supply noise
  - Identify the circuit exposed to the noise
  - Identify circuits very sensitive to supply noise
  - Separate sensitive circuits from large noise sources
  - Evaluate the margin impact of the noise
- Minimize supply-to-supply coupling
  - Inductive coupling between bond wires and traces
  - Shared ground bond wires and traces
- Worst supply noise occurs during state transition, not in active states
- Example: Advanced power management of mobile memory system
  - Several power states
  - Quick exit and entry
  - Critical transition: P3 → P4
- Power transition can generate large noise transients on the power supply rails
- The supply noise transient results in large power-supply induced jitters
Complete Link Analysis

- Channel ISI, reflection, crosstalk
- Power supply noise and induced jitter,
- Deterministic and random device jitter and noise
- Transceiver bandwidth limitations
- Noise of transmitter and receivers and clocks
- Jitter correlations and amplifications
Emerging Memory Interfaces

- Four emerging memory interfaces
  - DDR3/L/U (1.6 Gbps) and DDR4 (3.2 Gbps)
    - Desktop and workstations
  - LPDDR3 (2.133 Gbps) and LPDDR4 (4.266 Gbps)
    - Mobile and Tablet
  - GDDR5 (7 Gbps) / HMC (10, 12.5, 15 Gbps)
    - Graphics and main memory
  - WideI/O2 (800 Mbps), HMB
    - Mobile systems

- These interfaces represent different approaches to address the bandwidth, power, and area challenges

- The channel and the system environment are different
  - Channel length, Tx swing, DRAM packaging
Evolution of DDR

<table>
<thead>
<tr>
<th>Variables</th>
<th>SDRAM</th>
<th>DDR1</th>
<th>DDR2</th>
<th>DDR3</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD/VDDQ/VDP</td>
<td>3.3/2/5</td>
<td>2.5</td>
<td>1.8</td>
<td>1.5/1.5/-</td>
<td>1.2/1.2/2.5</td>
</tr>
<tr>
<td>Data Rate (Mbps)</td>
<td>166</td>
<td>400</td>
<td>800</td>
<td>2.133</td>
<td>3200</td>
</tr>
<tr>
<td>Clock</td>
<td>Single ended</td>
<td>Differential</td>
<td>Differential</td>
<td>Differential</td>
<td>Differential</td>
</tr>
<tr>
<td>Strobes</td>
<td>unsupported</td>
<td>Single ended</td>
<td>Single ended or Differential</td>
<td>Differential</td>
<td>Differential</td>
</tr>
<tr>
<td>Vref</td>
<td>N/A</td>
<td>External</td>
<td>External</td>
<td>Ex/Internal</td>
<td>Ex/Internal*</td>
</tr>
<tr>
<td>ODT</td>
<td>unsupported</td>
<td>unsupported</td>
<td>supported</td>
<td>supported</td>
<td>supported</td>
</tr>
<tr>
<td>Interface</td>
<td>LVTTL</td>
<td>SSTL</td>
<td>SSTL</td>
<td>SSTL</td>
<td>PODL</td>
</tr>
</tbody>
</table>

- Latest features
  - Shrinking supply
  - Point-to-point with matching termination
  - PODL with DBI
  - Internal Vref generation

* External for CA
Main Memory Channel

- No major improvement in the passive channel
  - FR-4 board, connector, device Ci
- Signal integrity issues at higher data rates limit the number of DIMM
  - Direct attached channel
  - FBDIMM (Fully buffered DIMM) and RLDIMM (Reduced load DIMM)
- Clock and Command/Address topologies and termination changed
  - Minimize stub length: Tree to fly-by topology
  - On board to module termination

Ref: Intel® Xeon® Processor 500 Series (Nehalem) DDR3 DIMM System-level Validation Results
PODL Signaling and Supply Noise Tracking

- Data Bus Inversion: one DBI pin per byte
  - DC: Limit the number of DQ lines per byte driving a Low to 4
  - AC: Number of bits switching within a byte not to exceed 4
- One reference shared between multiple pins
  - Coupling to supply network different from data
  - Couple supply noise to VREF over the frequencies where PDN peaks
- Most of the AC noise from the transmitter
  - Not tracked by the VREF at the receiver
Block Diagram of the DDR Interface

- Supply Partitioning to control noise and its impacts
  - The output drivers and front end of the receivers are on separate supply: VDDIO or VDDQ
  - The OMUX and other pre-driver stages are on VDDR
  - The clock distribution and PLL are on separate supplies
  - The partitioning are optimize using detailed on-chip and off-chip power integrity analysis

- Minimize supply-to-supply coupling
  - The supplies are separated at chip, package and even at board levels.
## Evolution of LPDDR

<table>
<thead>
<tr>
<th>Variables</th>
<th>LPDDR1</th>
<th>LPDDR2</th>
<th>LPDDR3</th>
<th>LPDDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD1, VDD2, VDDQ (V)</td>
<td>1.8</td>
<td>1.8/1.2/1.2</td>
<td>1.8/1.2/1.2</td>
<td>1.8/1.1/1.1</td>
</tr>
<tr>
<td>Data Rate (Mbps)</td>
<td>400</td>
<td>1066</td>
<td>2133</td>
<td>4266</td>
</tr>
<tr>
<td>CA</td>
<td>SDR</td>
<td>DDR</td>
<td>DDR</td>
<td>SDR</td>
</tr>
<tr>
<td>Clock</td>
<td>Single ended</td>
<td>Differential</td>
<td>Differential</td>
<td>Differential</td>
</tr>
<tr>
<td>Strobes</td>
<td>Single ended</td>
<td>Differential</td>
<td>Differential</td>
<td>Differential</td>
</tr>
<tr>
<td>Vref</td>
<td>External</td>
<td>External</td>
<td>External</td>
<td>Ex/Internal</td>
</tr>
<tr>
<td>ODT</td>
<td>unsupported</td>
<td>Unsupported</td>
<td>supported</td>
<td>supported</td>
</tr>
<tr>
<td>Interface</td>
<td>SSTL</td>
<td>HSUL</td>
<td>HSUL/PODL</td>
<td>LVSTL</td>
</tr>
</tbody>
</table>

- Latest features
  - Supply voltage shrinking
  - Internal reference voltage generation
  - Far-end termination
  - Reduced swing
LPDDR3/LPDDR4: I-V Characteristics

- Transmitter nonlinearity can affect the system performance
PoP Memory System

- PoP structure widely used in mobile devices
- Supply noise and package crosstalk are the major challenge to run at high data rates
  - Improve package design and wirebond length
  - Minimize PSIJ: Improve circuit sensitivity to supply noise
LPDDR3 / LPDDR4: Eye Diagrams

- LPDDR3: use of weak termination (240Ω → 120 Ω)
- LPDDR4: Smaller Ci improves margin
**Evolution of GDDR and HMC**

<table>
<thead>
<tr>
<th>Variables</th>
<th>GDDR1</th>
<th>GDDR2</th>
<th>GDDR3</th>
<th>GDDR4</th>
<th>GDDR5</th>
<th>HMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD (V)</td>
<td>2.5</td>
<td>1.8</td>
<td>1.5</td>
<td>1.5</td>
<td>1.35</td>
<td>1.2</td>
</tr>
<tr>
<td>Data Rate (Mbps)</td>
<td>0.3-0.9</td>
<td>0.8-1.0</td>
<td>0.7-2.6</td>
<td>2.0-3.0</td>
<td>3.6 - 7</td>
<td>10-15</td>
</tr>
<tr>
<td>DQ</td>
<td>Single ended</td>
<td>Single ended</td>
<td>Single ended</td>
<td>Single ended</td>
<td>Single ended</td>
<td>Differential</td>
</tr>
<tr>
<td>Clock</td>
<td>Single ended</td>
<td>Differential</td>
<td>Differential</td>
<td>Differential</td>
<td>Differential</td>
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<td>Strobes</td>
<td>Single ended, DQS</td>
<td>Differential, DQS, DQSB</td>
<td>WDQS, RDQS, Uni-directional</td>
<td>WDQS, RDQS, Uni-directional</td>
<td>WDQS, RDQS, Uni-directional</td>
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<tr>
<td>Interface</td>
<td>SSTL</td>
<td>SSTL</td>
<td>PODL</td>
<td>PODL</td>
<td>PODL</td>
<td>SerDes</td>
</tr>
</tbody>
</table>

- **GDDR new features**
  - Data bus inversion (DBI)
  - Address bus inversion (ABI)
- **HMC**: Hybrid Memory Cube
  - SerDes: Tx and Rx equalization
HMC Memory System

- Interface is SERDES
- Data rate: 10 to 15 Gbps
- Channel is short
  - Point to point and differential
  - Uni-directional and double-terminated
- EQ architecture: TX EQ, RX CTLE and DFE
- AC coupling: Optional
Channel Responses w/ and w/o CTLE

- Channel length and Ci increase attenuation
- Channel +CTLE response shows -14 dB of attenuation
- Stripline routing can further improve the crosstalk
- Significant pre (≈20%) and post cursor (>50%) ISI's
• DFE Equalization opens eye significantly
• Major contributors to margin loss
  – Channel (ISI +crosstalk) is major : 26 ps
  – Device noise and jitter: 21 ps
  – Timing Margin : 20 ps at low BER
Conclusions : Signal and Power Integrity

• Increased data rate and reduced voltage supply
  – Tighter timing and voltage margin
• Topology and channel selections
  – Voltage margin improvement using simple equalization techniques
  – Timing improvement with better tracking between data and strobe
• To optimize the overall design and ensure robust link operation,
  – critical to take into account all major system impairments early
  – off-chip components, on-chip circuitry system architecture
• The power-state transition creates
  – large noise transients on the power supply rails
  – results in large power-supply induced jitter
• Cost sensitivity
  – Shortened time window for sign-off
  – Debugging failure is more difficult
I would like to acknowledge the Rambus SI/PI engineers for their contributions and many helpful discussions over the years.
Outline of Tutorial

- DRAM review [John]
- Conventionally packaged interfaces [John]
  - Evolution of standard interfaces
  - Signaling and clocking at peak bandwidth
  - Bandwidth variation
- 3D Packaging for Memory Applications [Ming]
  - Traditional 3D Packaging Technologies
  - New TSV Based 3D Packaging Technologies
- Signal and power Integrity [Wendem]
  - Signal and power integrity challenges
  - Memory interface analysis methodology
  - Main features of memory interfaces
  - Comparison of emerging standards-based solutions
- Conclusion and Final Comparison [John]
## Qualitative Tradeoffs Across Interface Solutions

<table>
<thead>
<tr>
<th></th>
<th>DDRn</th>
<th>LPDDRn</th>
<th>3D</th>
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<tbody>
<tr>
<td></td>
<td>DDR3</td>
<td>DDR4</td>
<td>LPDDR2</td>
</tr>
<tr>
<td>Cost</td>
<td>+++</td>
<td>-</td>
<td>++</td>
</tr>
<tr>
<td></td>
<td>Mainstream</td>
<td>Not avail</td>
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<tr>
<td>Pwr Efficiency</td>
<td>-</td>
<td>+</td>
<td>++</td>
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<td>DBI, V scaling</td>
<td>Burst mode, HSUL</td>
<td>Burst mode, PODL</td>
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<tr>
<td>BW</td>
<td>++</td>
<td>+++</td>
<td>-</td>
</tr>
<tr>
<td>Controller complexity</td>
<td>++</td>
<td>+</td>
<td>++</td>
</tr>
<tr>
<td></td>
<td>Transaction gaps</td>
<td>New features</td>
<td>Power state transition</td>
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<tr>
<td>SI/PI</td>
<td>+</td>
<td>++</td>
<td>++</td>
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<tr>
<td></td>
<td>Mulit-rank, long channel</td>
<td>DBI, more pt. to pt.</td>
<td>Short</td>
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<tr>
<td>Thermal</td>
<td>++++</td>
<td>+++</td>
<td>++</td>
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<tr>
<td></td>
<td>Topology</td>
<td>Higher BW</td>
<td>POP, mobile</td>
</tr>
<tr>
<td>Form Factor</td>
<td>+</td>
<td>+</td>
<td>++</td>
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</table>
Even “Ideal” Interface has Finite Value to System

<table>
<thead>
<tr>
<th>Power @ Unit Performance</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>C/GPU Core</td>
<td>Memory Controller</td>
</tr>
</tbody>
</table>

Hypothetical I/O:
- Unlimited bandwidth
- Zero Power

- OR -

C/GPU Core | Memory Controller | DRAM Core

Finite power ↓ at same performance

Finite performance ↑ at same power

Value depends on relative power/performance of different components
• Low margins dictate high volumes
  – Any DRAM type must have significant % of market to be viable
• Multi-sourcing amortizes investment, risk
  – OEM requires multiple DRAM vendors
  – DRAM vendor needs devices to ship into multiple applications
• Price discrimination
  – DRAM devices are speed binned to monetize high & low end
  – Same GPU can ship with GDDR or DDR in high/low end systems
• This all makes abrupt technology transitions difficult
  – Even evolutionary transitions face these challenges
  – Historically, controllers are bimodal across generations
Summary

• Conventional interfaces must (will) continue evolving
  – Lower active power, lower effect power under workload
  – Sometimes needed in coordination with 3D integrated devices

• 3D integration offers disruptive interface benefits
  – Dramatic I/O efficiency improvement
  – New capabilities such as server capacity aggregation

• 3D faces uphill economic battle for market adoption
  – Value to system must justify cost (vs. alternatives)
  – Will start as niche in high-value applications:
    Server memory, HPC, later in high-end mobile
  – Slow trickle down to more mainstream applications