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SANTA CLARA CONVENTION CENTER

World's First LPDDR3 Enabling for Mobile Application Processors System

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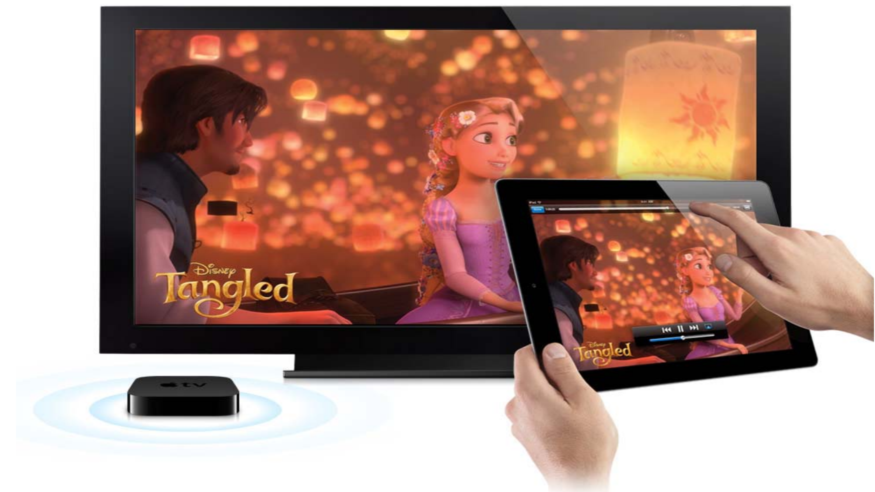
UBM Electronics

Contents

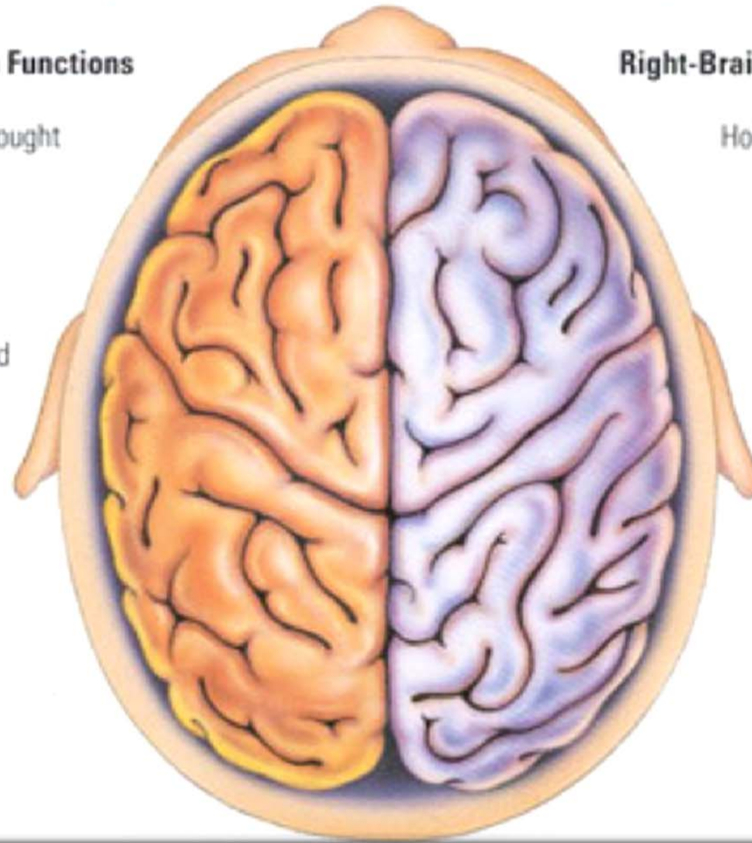
- Introduction
- Problem Statements at Early mobile platform
- Root-cause, Enablers
  - SCP (Single Chip Package)
  - POP (Package-On-Package)
- Enabled Platform Prediction and Results
- Summary

Mobile World : Joyful & Happy

Mobile Life / See & Enjoy



Mobile EQ Upgrade



Left	Right
Speech	Image
Text	Graphic
Numbers	Color

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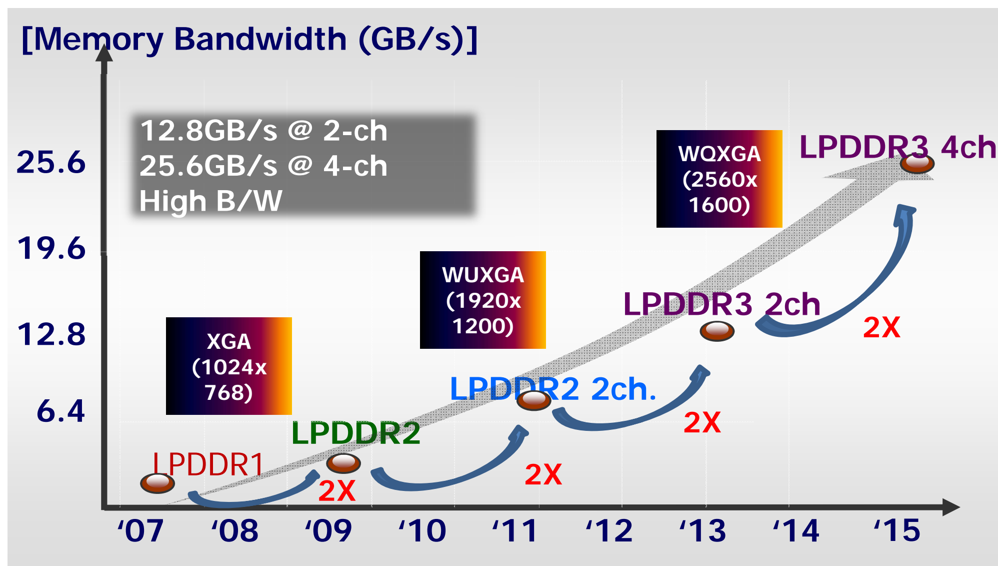
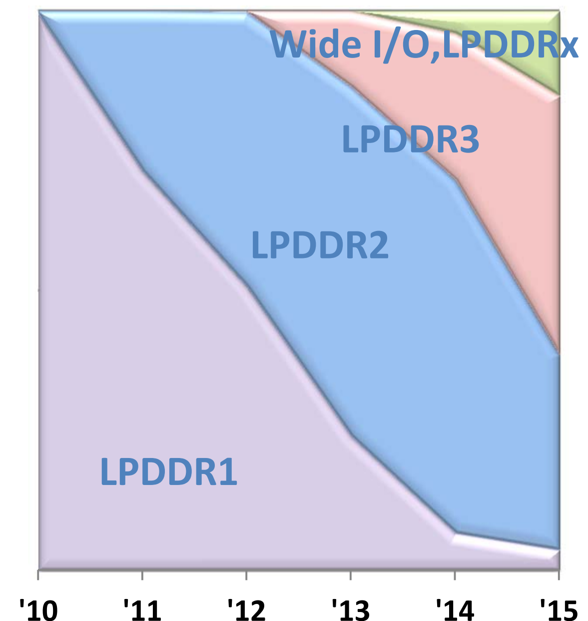
Mobile DRAM BW Requirements

- Mobile DRAM B/W requirement is growing very fast
  - MDDR('05, 1X) → LPDDR2('10, 2X) → LPDDR3('12, 4X)
  - Key driving factors : High graphic resolution Enc./Dec., 3D graphic, Web…

Mobile DRAM Bandwidth Requirements



Technology Transition



LPDDR3 is the right solution to evolve the mobile generation

Samsung LPDDR3 features

- LPDDR3 specification table-1
  - Evolutionary solution from LPDDR2 : Easy adoption for industry

	Item	LPDDR2	Samsung LPDDR3
Feature	Process	-	3X nm
	Density	-	4Gb
	Max. B/W(1/2-Ch)	4.3/8.5	6.4/12.8
	CLK/DQS scheme	Diff., Bi-dir.	←
	ADD/CMD scheme	DDR, Single-end.	←
	Data scheme	DDR, Single-end.	←
	I/O Interface	HSUL_12V	←
	Burst Length	4, 8, 16	8
	Burst Type	Seq., Int.	Seq.
	No Wrap	Support(BL4)	No support
	Organization	x16/x32	←
Addressing	Address (4Gb X32)	BA0~BA2/ RA0~RA13 /CA0~CA9	←

Samsung LPDDR3 features

- LPDDR3 specification table-2

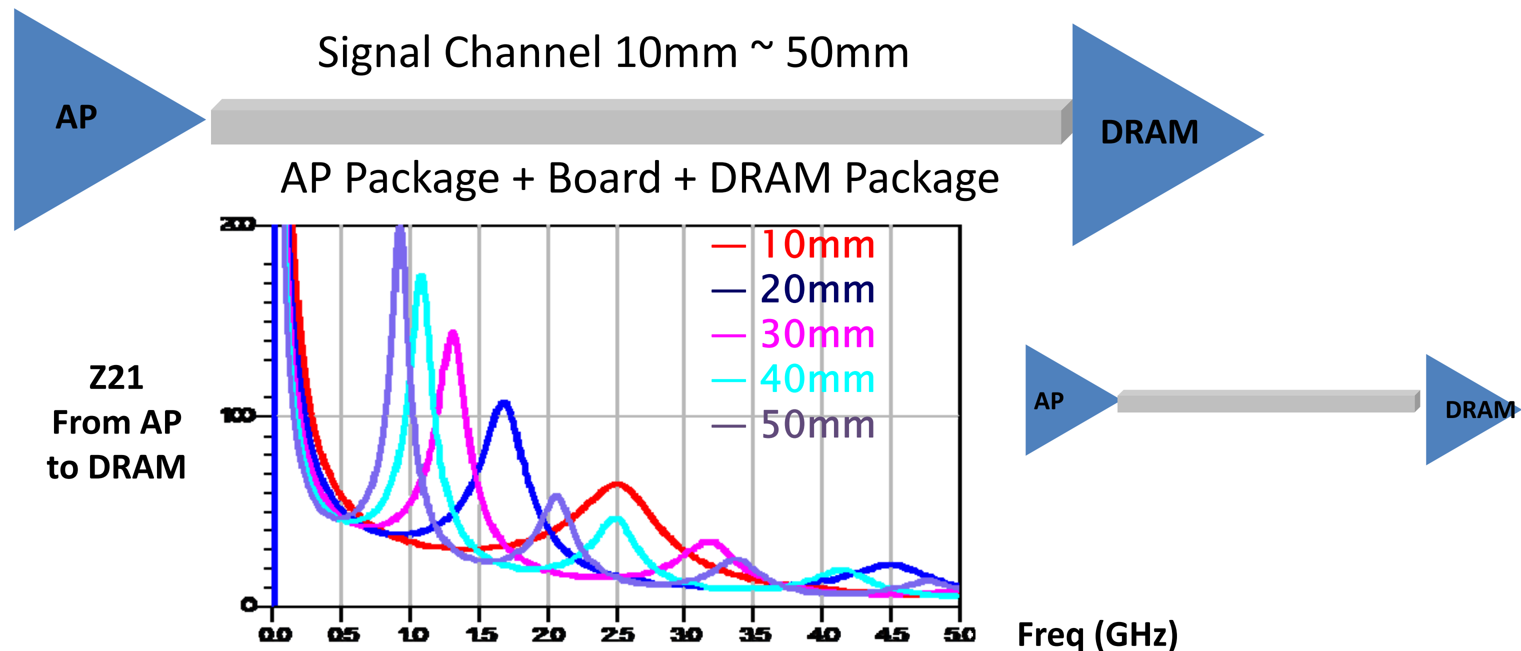
*Note : 1)Target spec at 800Mbps, 2)Target spec at 1600Mbps

	Item	LPDDR2	Samsung LPDDR3
Power	VDD1/VDD2/VDDQ/VDDCA	1.8V/1.2V/1.2V/1.2V	←
AC Parameter	Speed bin(Mbps)	667/800/1066	1333/1600
	RL/WL	3/1, 4/2, 5/2, 6/3, 7/4, 8/4	6/3, 8/4, 9/5, 10/6, 11/6, 12/6
	nWR	3~8	6,8,9,10,11,12
	tIS/tIH tDS/tDH	290/290*1) 270/270*1)	155/155*2) 150/150*2)
	In/Out. Cap	CA : 1.0 ~ 2.0pF (Die) DQ : 1.25 ~ 2.5pF (Die)	CA : 0.75 ~ 1.5pF (Die) DQ : 1.0 ~ 2.0pF (Die)
	VIH/VIL	VREF +/- 220mV (AC) VREF +/- 130mV (DC)	VREF +/- 150mV (AC) VREF +/- 100mV (DC)
Special Function	PASR	Support	←
	TCSR	Support	←
	Deep Power Down	Support	←
	ZQ Calibration	Support	←
	DQ Calibration	Support	←
	CA Calibration	N/A	Support
	Write Leveling	N/A	Support
	ODT	N/A	Support(POD Type)

Several functions are implemented to achieve 1600Mbps operation

Common Mobile Channel

- Common mobile channel
  - Typical channel length from AP die to DRAM die : 10mm to 50mm
  - Open Termination for lower power consumption



Channel acts like λ/4 resonator over 800MHz

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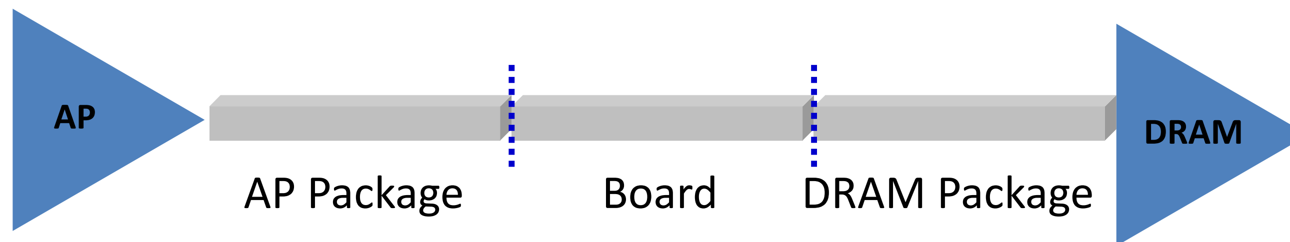
Challenges for HSUL 12 with LPDDR3

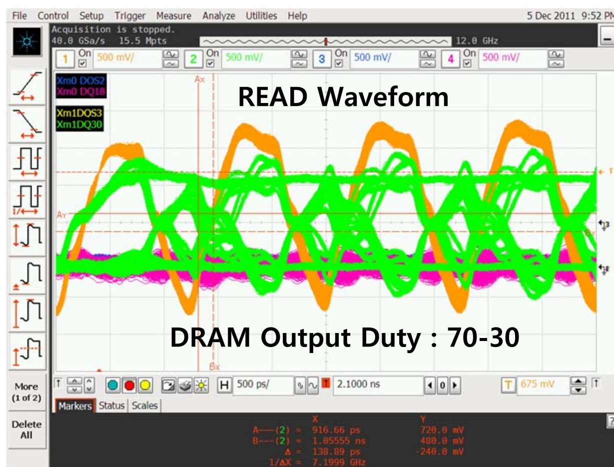
- Channel Characteristics
  - Channel : λ/4 resonator near operation frequency
  - Full swing from VSSQ to VDDQ
  - Small energy couplings can induce large distortions
  - Need full channel characterization to get accurate estimations
- Previous Modeling Method



  - Divide the models to model the channel efficiently
  - Models are merged at the transient simulation engine
  - Issues
    - Interaction between models such as inductive current loop
    - Different frequency information for each model

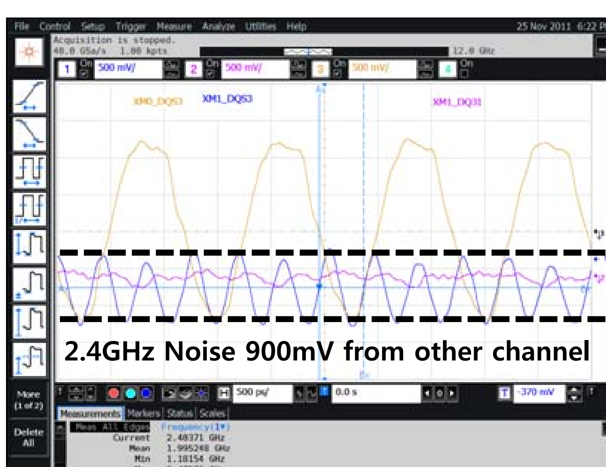
Memory Problem Statements

In-Channel Coupling+ISI



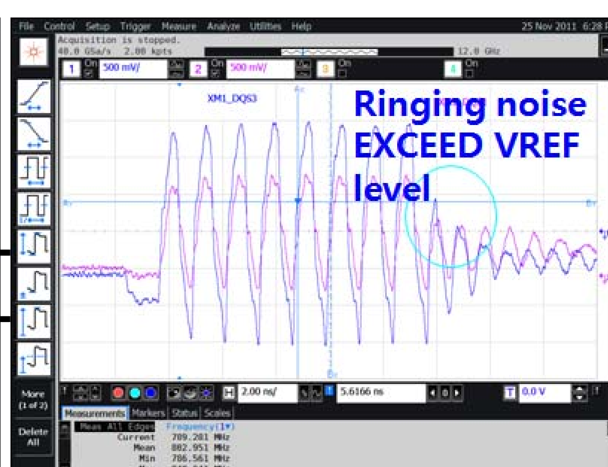
* Xm1 DQS3 Xm1 DQ31

Inter-Channel Coupling



* Xm1 DQS3 Xm1 DQ31
* Xm0 DQS3

READ Postamble Ringing

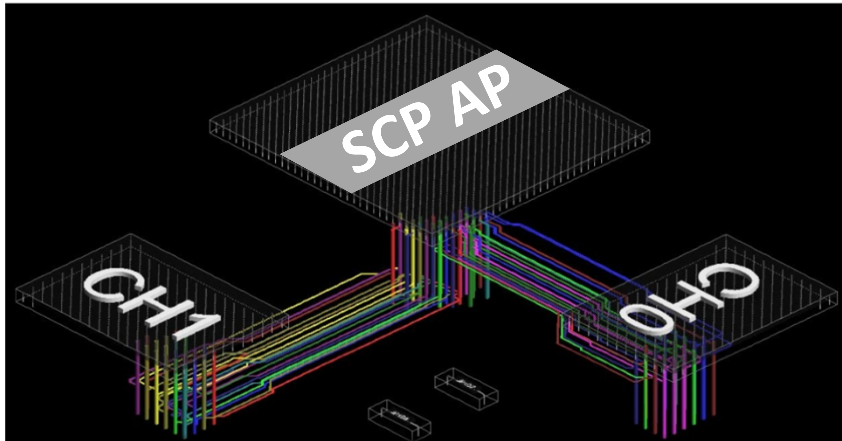


* Xm1 DQS3 Xm1 DQ31

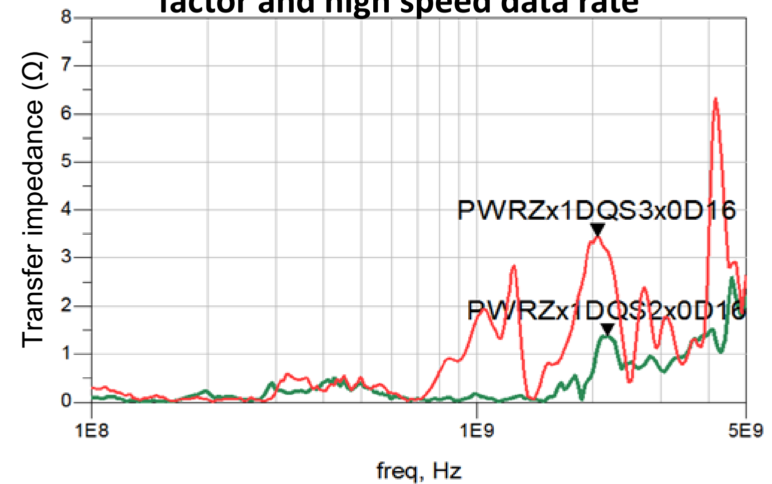
- **Problem Statement:** LP DDR3 failure due to low margin
- **Key Observation:** 3D effect + Channel lengths electrically long >~ λ/4 (Tp>400ps) in multi-Gbps signaling
- **Expected major failure causes:**
  - Crosstalks: In-byte, Other-byte, Inter-channel
  - Read Postamble Ringing : Ringing can cause logic failure at next READ operation
  - **First design for EVT0:** Highly inductive PDN on MB, 3D effects including imperfect ground/ power distribution

Problem : Inter-channel Coupling

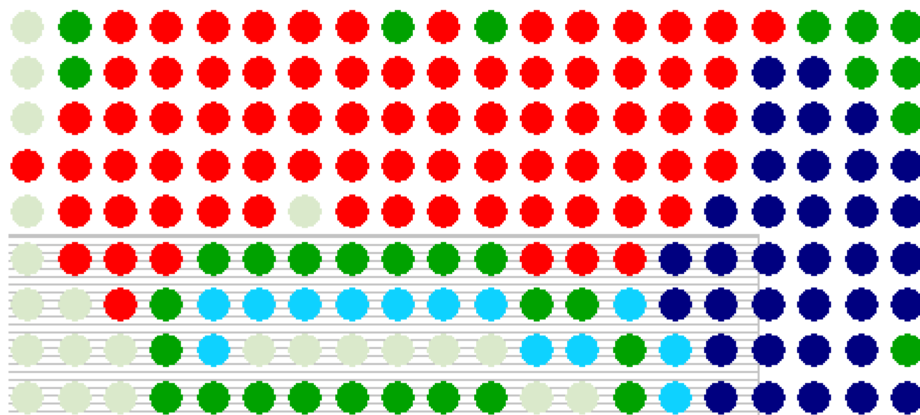
- Coupling analysis based on 3D structure



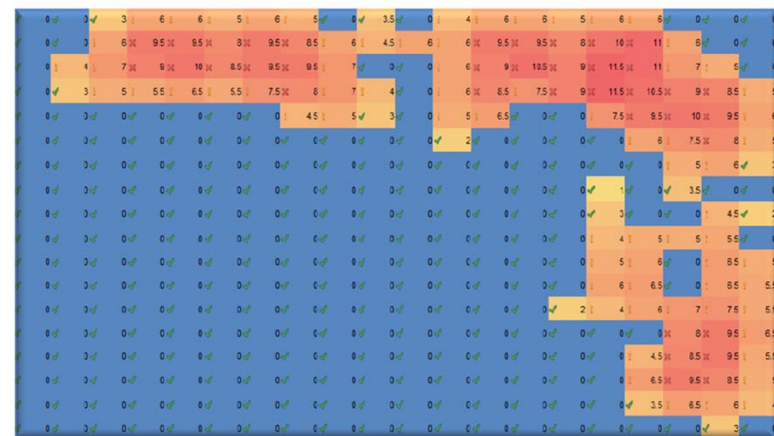
- Severe inter-channel crosstalk depending on small form factor and high speed data rate



First Ball Map ● Ground ● CH0 Signals ● CH1 Signals



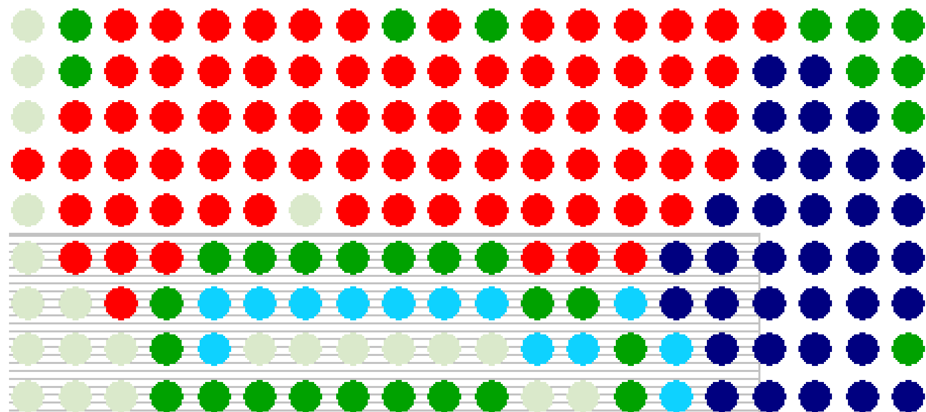
Aggressor weighting diagram

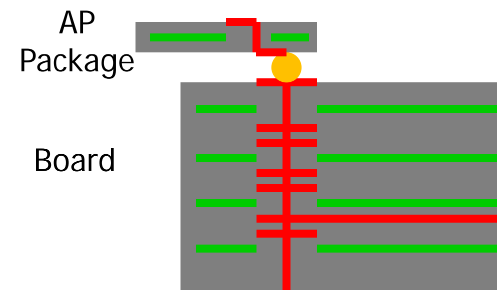


Need Ball map improvement in order to reduce inter-byte/channel X-talk

Problem : Return Current Path

- large inductive loop size in SCP Package and Board
  - Far ground ball from each signal
  - Sharing the ground balls with many signals → large mutual effect
  - Long via lengths & deep signal layer from AP package → inductive discontinuity

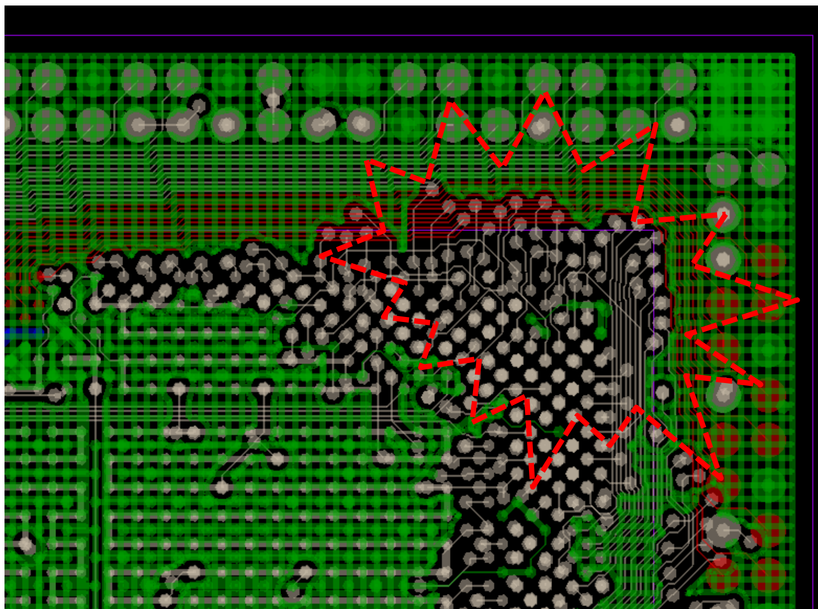




Re-arrange the signal layers in Mobile reference Board

Problem : Slots under Signal Bump

- Slots under signal bump and break-out area in POP package
  - Some byte has not enough ground plane
  - Slots increase signal coupling and degrade signal quality

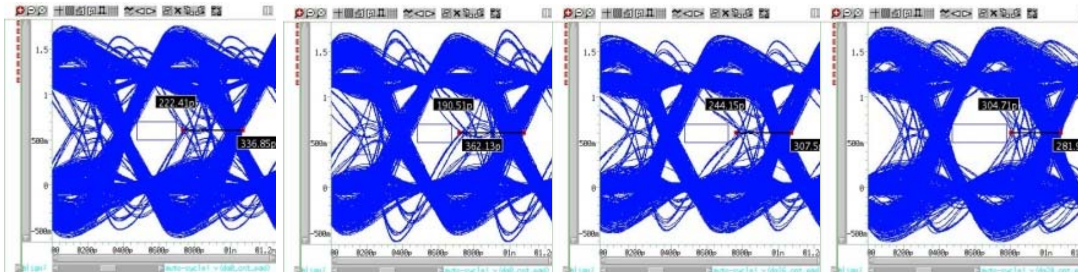


Tune the Package design to remove slots

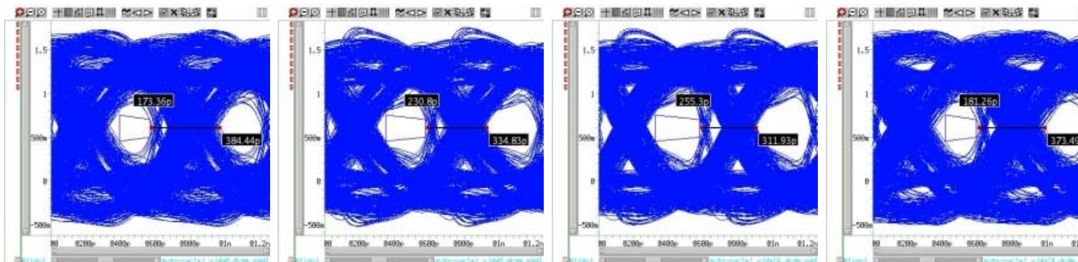
Simulation Results with Merged Model

- Condition : LPDDR3 1600Mbps without Termination in SCP
  - To operate at 1600Mbps, 325ps or more margin is needed (50% UI)
  - Signals are degraded by couplings from various sources
    - Planar crosstalk effects / 3D structural effects from inductive coupling

Byte0 Byte1 Byte2 Byte3



Read
Min. margin
191ps

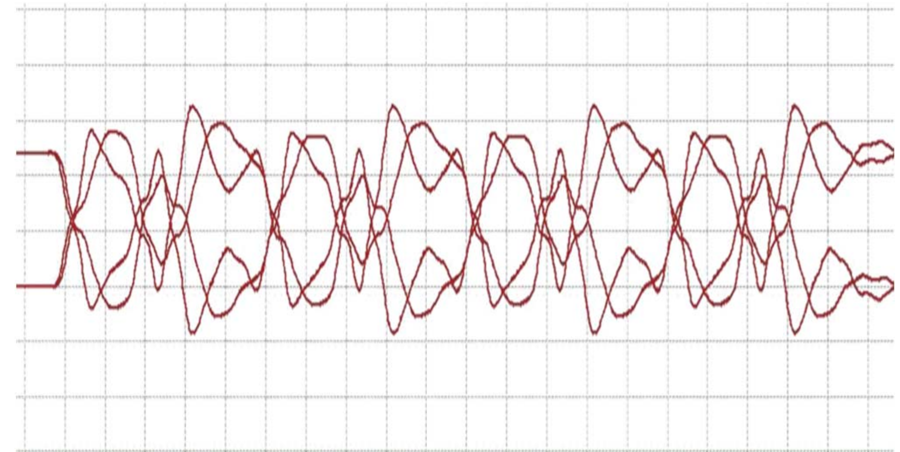


Write
Min. margin
173ps

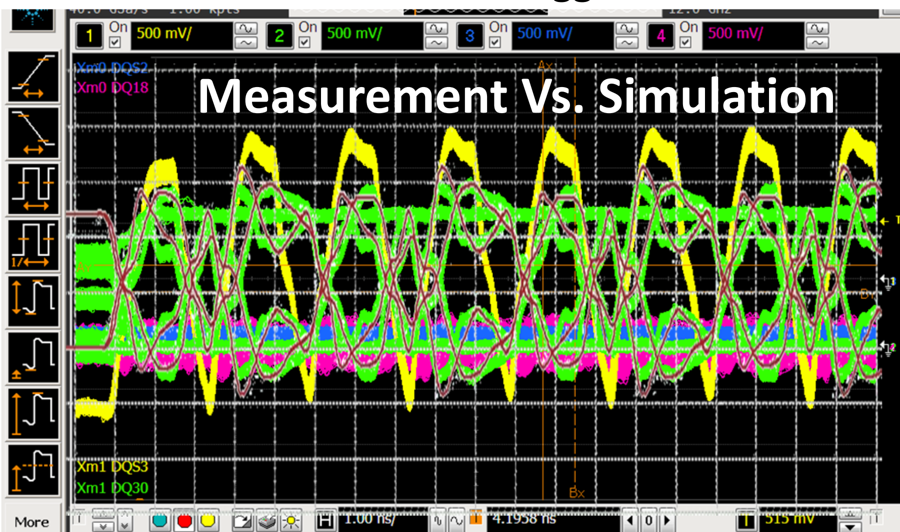
1600Mbps operation could not be possible

Correlation btw Sim. & Measurement

Measurement with 7 aggressors



Simulation waveform with 7 aggressors



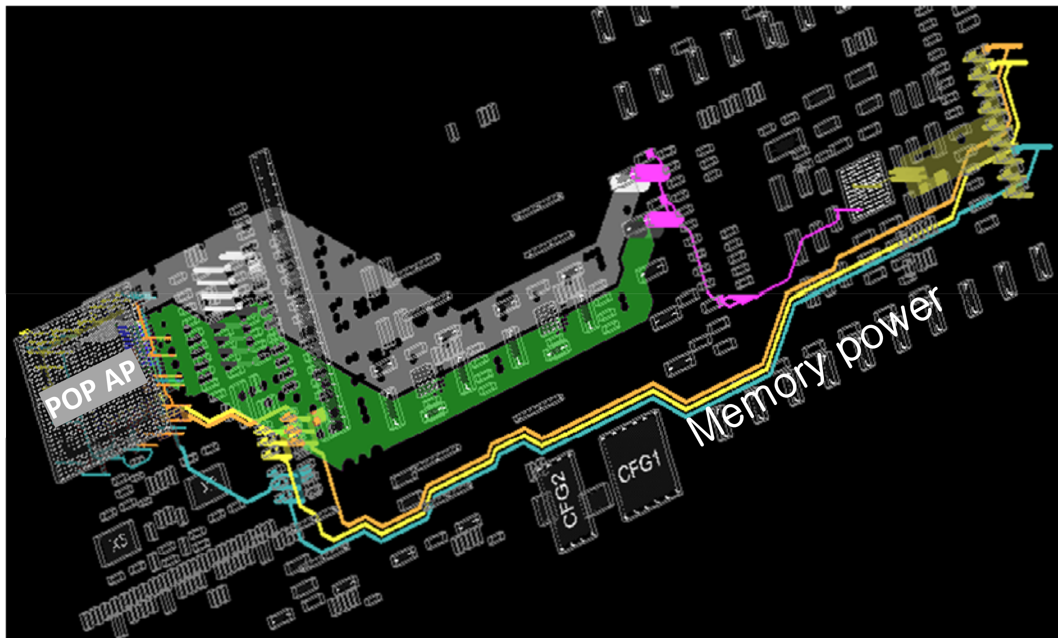
Simulation matches up with measurement results using 3D-merged model

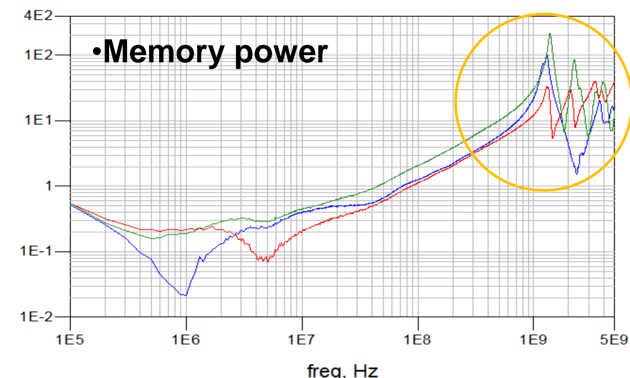
Simulation correlated with measurement and reflects all channel effects

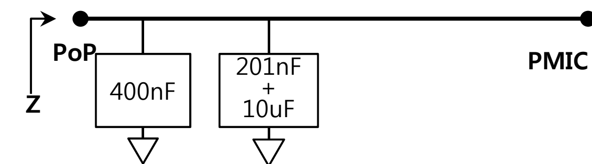
Problem : Inductive PDN

- PDN was too inductive at POP SMDK Board
  - Inductive PDN caused large voltage noises
  - This problem was root-caused via VNA measurement

Power distribution network of POP Mobile platform regarding LPDDR3





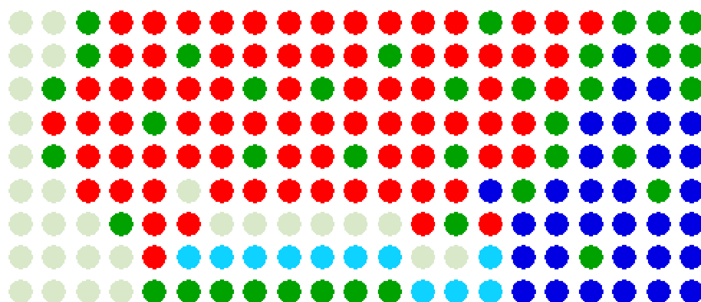


Need to optimize Board PDN

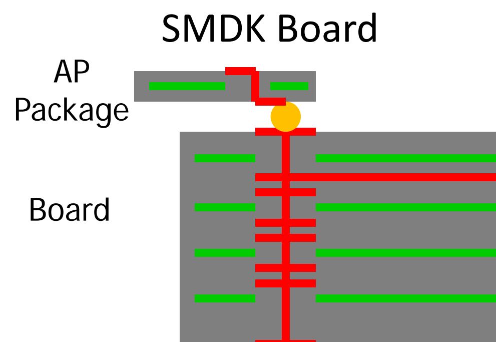
Enabled Platform - 1

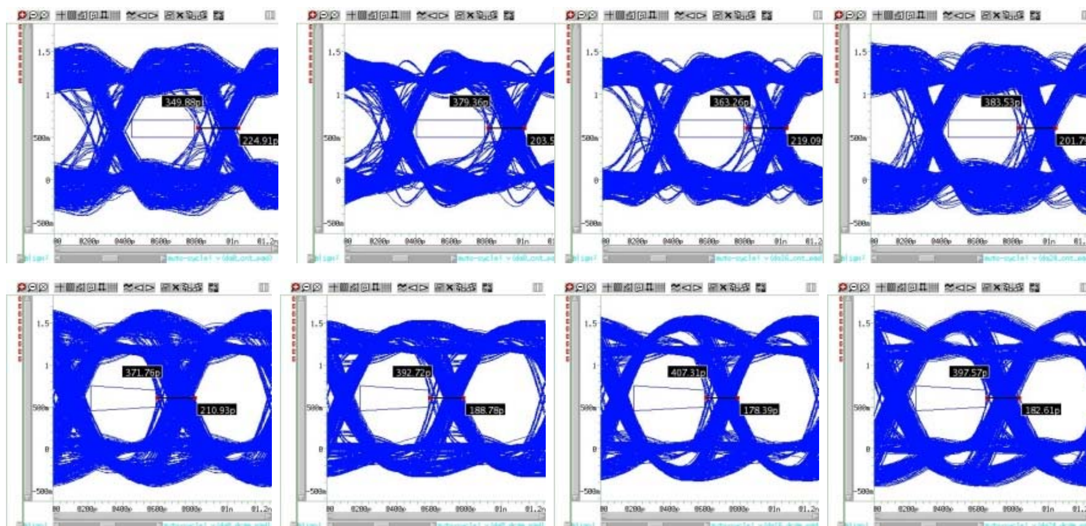
- Simulation with enablers – Ball map & Board re-design

Enabled Ball map ● Ground ● Signals ● Signals



SMDK Board





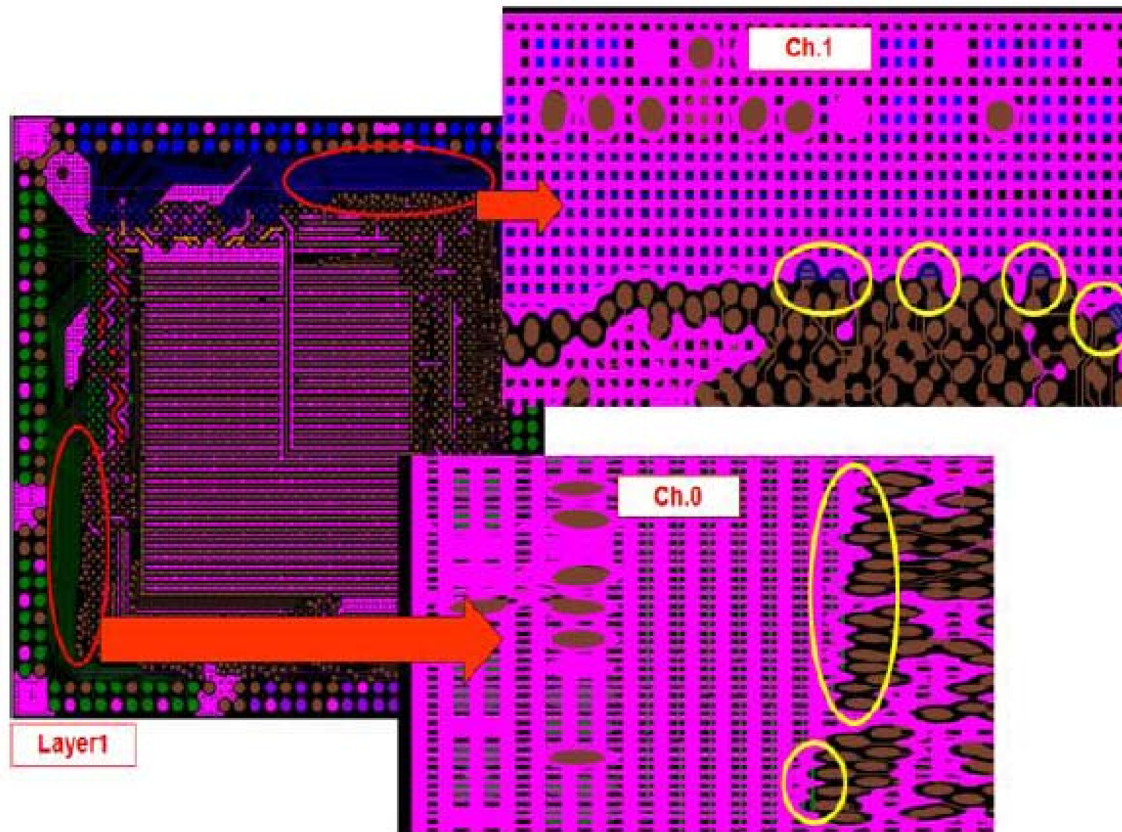
Read margin
191ps → **350ps**
(+159ps)

Write Margin
173ps → **372ps**
(+199 ps)

Through enablers, 1600Mbps operation looks feasible

Enabled Platform - 2

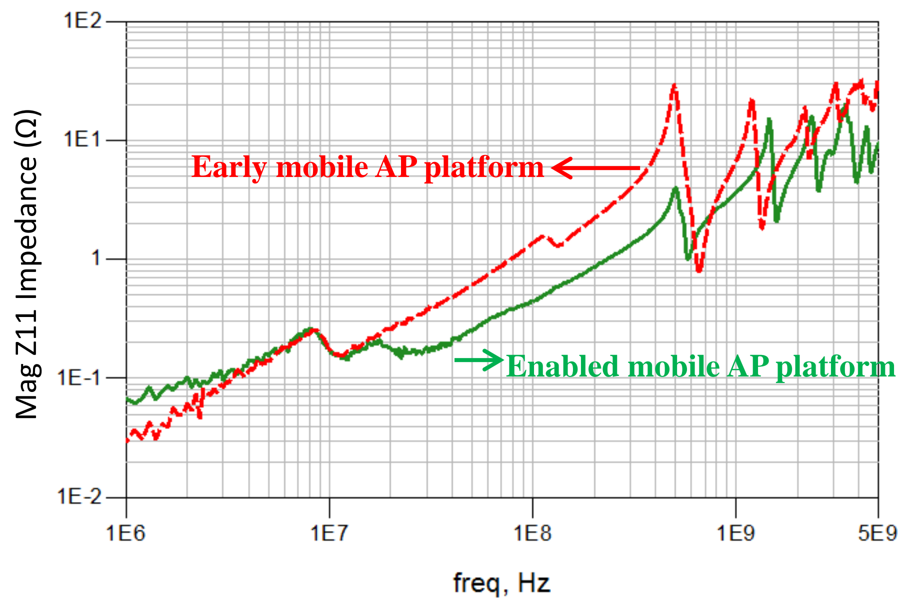
- Enforcement of reference plan for data signals in POP

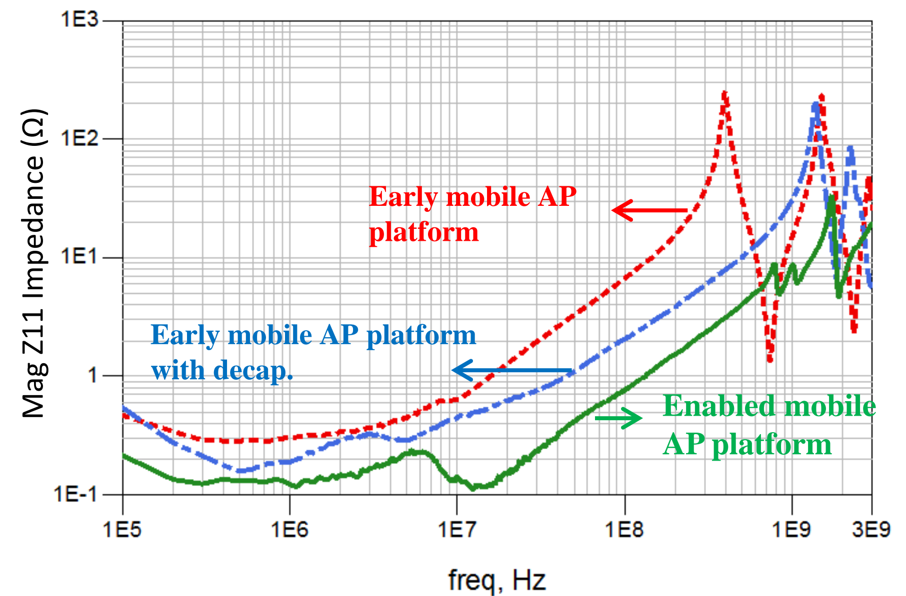


The electrical performance is improved about 48ps timing margin by this change

Enabled Platform - 3

- Power Delivery Network (PDN) Optimization





***** Measurement***

- Power-on

- probe point: around AP package ball

Lower inductive PDN design is needed to support stable power

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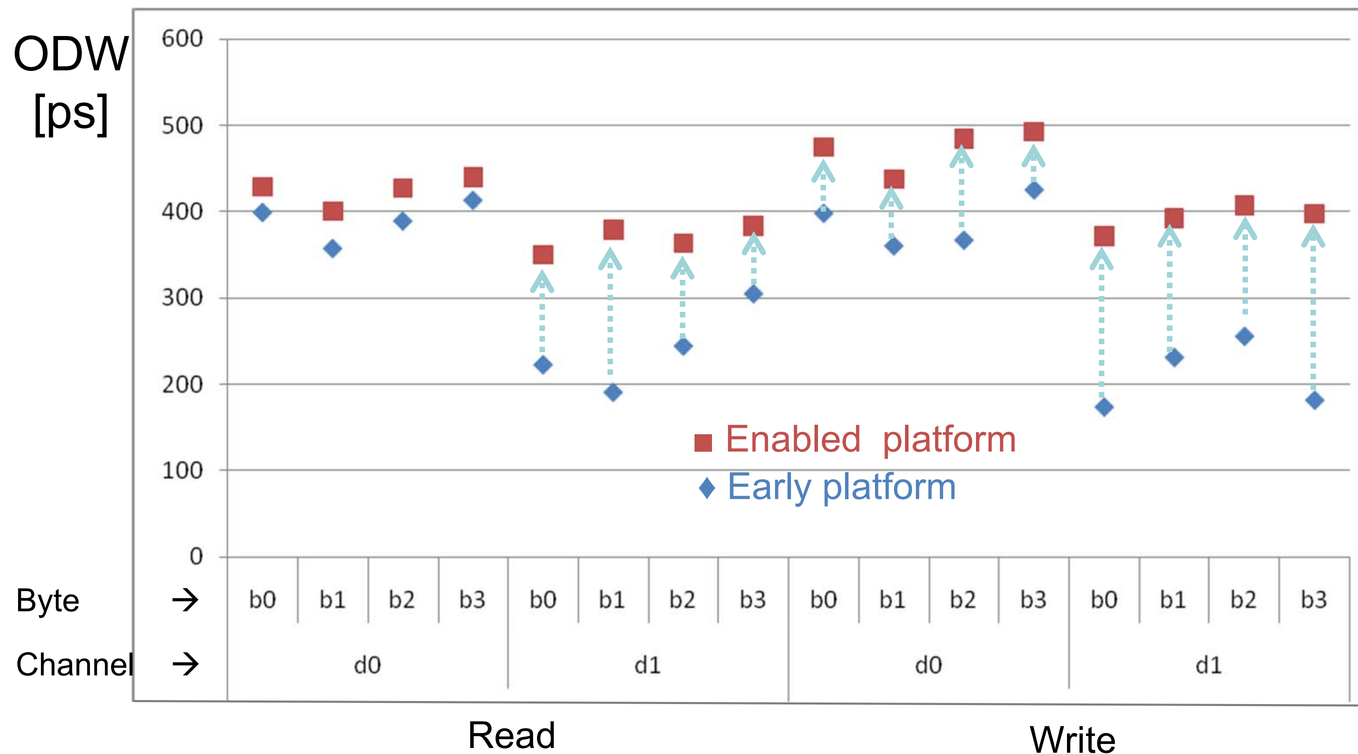
Result of Enabled system

- Timing margin improvement comparison between Early and Enabled platform



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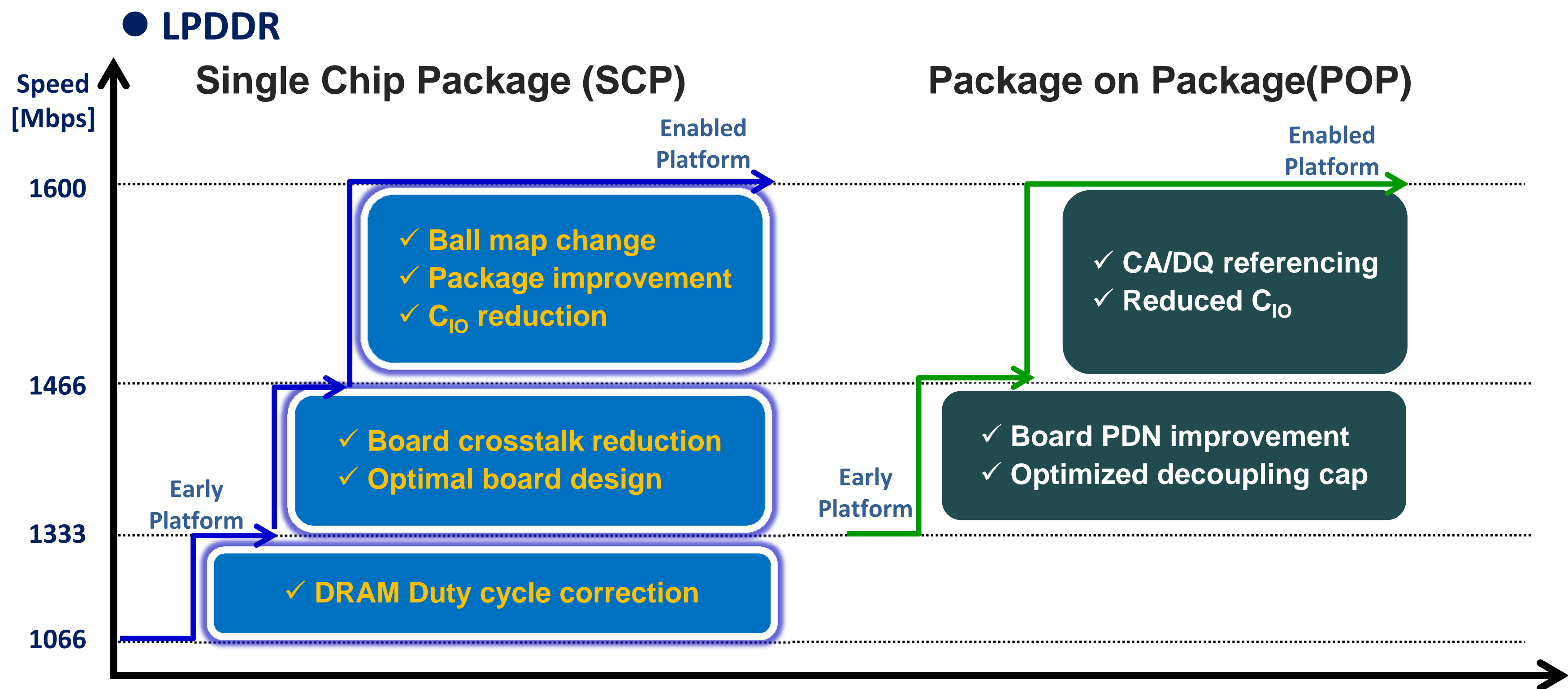
Summary - 1

- Key speed enablers on each LPDDR3 data rate



Summary - 2

- Mobile AP has foremost new high speed LPDDR3
- First test chip initially failed to achieve POR data rate in the mobile platform
- Root-caused SI/PI phenomenon using accurate simulation and measurement
- This work presents robust platform I/O signaling solutions to enable world's first LPDDR3 in mobile AP platform