DDR4 Board Design and Signal Integrity Verification Challenges
Outline

• Enabling DDR4
  – Pseudo Open Drain Driver - Benefit
  – POD – SI effects
  – VrefDQ Calculation
  – Data Eye

• Simulating SSN
New Drive Standards – Difference

DDR4 (Pseudo Open Drain)

DDR3 (Stub Series Terminated Logic)
New Drive Standards – Why?

- Current still flows when driving low
New Drive Standards – Why?

- No current draw when driving a high
Power Savings with DBI

- Ensure more 1’s than 0’s with POD
- If more than 4 bits in a byte are 0, toggle bits
- DBI shared with DM => only one feature enabled
- DBI pin is I/O (effects both reads and writes)
Implications for SI

• What does asymmetric termination mean for reference threshold voltage ("center voltage of eye")?
  – Take average voltage of high and low at receiver
  – Assume a very short trace for sake of simple calculations
  – Assume balanced high and low drive strength

\[
\text{Rt} = \text{Termination Resistance} \\
\text{Zo} = \text{Transmission Line Impedance} \\
\text{Zd} = \text{Driver Output Impedance}
\]
When Driving High

\[ V_h = (V_{dd}) \left( \frac{R_t}{R_t + Z_d} \right) + \left( \frac{V_{dd}}{2} \right) \left( \frac{Z_d}{R_t + Z_d} \right) \]

When Driving Low

\[ V_l = \left( \frac{V_{dd}}{2} \right) \left( \frac{Z_d}{R_t + Z_d} \right) \]

\[ V_{avg} = \frac{V_h + V_l}{2} = \left[ \left( \frac{V_{dd}}{2} \right) \left( \frac{2R_t + Z_d}{R_t + Z_d} \right) + \left( \frac{V_{dd}}{2} \right) \left( \frac{Z_d}{R_t + Z_d} \right) \right] / 2 = \left[ \left( \frac{V_{dd}}{2} \right) \left( \frac{2R_t + 2Z_d}{R_t + Z_d} \right) \right] / 2 = \frac{V_{dd}}{2} \]
DDR4 – Center Voltage

When Driving High

\[ V_h = V_{dd} \]

When Driving Low

\[ V_l = V_{dd} \left( \frac{Z_d}{R_t + Z_d} \right) \]

\[ V_{avg} = \frac{V_h + V_l}{2} = \frac{1}{2} \left[ (V_{dd}) + \left( V_{dd} \right) \left( \frac{Z_d}{R_t + Z_d} \right) \right] \]

\[ = \left( \frac{V_{dd}}{2} \right) + \left( \frac{V_{dd}}{2} \right) \left( \frac{Z_d}{R_t + Z_d} \right) \]
DDR3 vs. DDR4 Vcent Comparison

- DDR3, Vcent = Vdd/2
  - Constant, regardless of setup

- DDR4, Vcent = f(Rt, Zd)
  - Varies from setup to setup
  - Varies from read to write
  - Varies across access to different DRAMs
Input Threshold Levels

- **DDR3**
  - Absolute $V_{ih}/V_{il}$ thresholds stayed **constant** in DDR3 across designs

- **DDR4**
  - Absolute $V_{ih}/V_{il}$ threshold levels can **change** in DDR4
Simple Comparison

- Controller $\rightarrow$ 50 Ohm Transmission Line $\rightarrow$ DRAM
- Vary DRAM’s ODT to see center level of eye
- 2400Mbps Datarate
DDR3 – Sweeping Rx ODT

- No change in Center of eye with ODT
• Eye center shifts with ODT change
Vref for a Device

• Need Precision programmable reference voltage
• Center voltage can vary across pins
• Individual Vref per pin may be too expensive
  – Silicon and power

• How to determine voltage used for all pins?
Determining Vref – “Avg”

- 8 bit device, one Vref resource
- Eye-center of bits different, as below

Option 1: Average of all signals
\[
\frac{800 + 750 + 730 + 725 + 720 + 710 + 705 + 700}{8} = 730\text{mV}
\]

Option 2: Average of extreme signals
\[
\frac{800 + 700}{2} = 750\text{mV}
\]
Margin Loss for a given bit

Margin Loss = $M_p - M_d = V_d - V_x$

Note: (The margin “loss” will be negative on the low side waveform in this case – i.e. a margin gain)
Average Margin Loss – Option 1

\[ Margin Loss = M_p - M_d = V_d - V_x \]

\[ V_d = \frac{\sum V_x}{n}. \text{ (Device Vref is average of all pins)} \]

\[
\text{Average Margin Loss} = \frac{\sum (V_d - V_x)}{n} \\
= \frac{\sum V_d}{n} - \frac{\sum V_x}{n} \\
= \frac{nV_d}{n} - V_d = 0
\]

As intuitively expected!
Average Margin Loss – Option 2

$$\text{Margin Loss} = M_p - M_d = V_d - V_x$$

$$V_d = \frac{V_{\text{max}} + V_{\text{min}}}{2}.$$  (Device Vref is average of extreme pins)

$$\text{Average Margin Loss} = \frac{\sum (V_d - V_x)}{n}$$

$$= \frac{(V_d - V_{\text{max}}) + (V_d - V_{\text{min}})}{n} + \frac{\sum_{x \neq \text{max, min}} (V_d - V_x)}{n}$$

$$= \frac{2V_d}{n} - \frac{(V_{\text{max}} + V_{\text{min}})}{n} + \frac{\sum_{x \neq \text{max, min}} (V_d - V_x)}{n}$$

$$= \frac{2}{n} \left( \frac{V_{\text{max}} + V_{\text{min}}}{2} \right) - \frac{(V_{\text{max}} + V_{\text{min}})}{n} + \frac{\sum_{x \neq \text{max, min}} (V_d - V_x)}{n}$$

$$= \frac{\sum_{x \neq \text{max, min}} (V_d - V_x)}{n}$$
Option 1 always has average margin loss of 0
Option 2 has average margin loss (on one side) of ≥ 0

Shouldn’t we choose Option 1?

No! Consider worst case pins.
Average Margin Loss – Comparison

Option 1: Average of all signals

730mV

730+68 = 798mV (Vinh)
730-68 = 662mV (Vinl)

Option 2: Average of extreme signals

750mV

750+68 = 818mV (Vinh)
750-68 = 682mV (Vinl)
### Average Margin Loss – Comparison

<table>
<thead>
<tr>
<th>Voltage (mV)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>800</td>
<td></td>
</tr>
<tr>
<td>750</td>
<td></td>
</tr>
<tr>
<td>730</td>
<td></td>
</tr>
<tr>
<td>725</td>
<td></td>
</tr>
<tr>
<td>720</td>
<td></td>
</tr>
<tr>
<td>710</td>
<td></td>
</tr>
<tr>
<td>705</td>
<td></td>
</tr>
<tr>
<td>700</td>
<td></td>
</tr>
</tbody>
</table>

- Assume eye height same at all pins,
  - Eye height of 260mV ($V_{center} \pm 130mV$)
  - (Not strictly true, but 800mV is still worst case)
- 800mV center signal swings between 670mV to 930mV

**Option 1**

- $730 + 68 = 798mV$ (Vinh)
- $730 - 68 = 662mV$ (Vinl)

**Option 2**

- $750 + 68 = 818mV$ (Vinh)
- $750 - 68 = 682mV$ (Vinl)
Do you really want to spread out the margin of your worst case signal to the non-critical signals?

- If worst case signals work, all other signals will work.
Vref for DDR4 DRAM

- Single Voltage, regardless of x4, x8 or x16

Figure 2. Vcent_DQ Variation to Vcent_DQ(midpoint)

The Vref_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent_DQ(midpoint), in order to have valid Rx Mask values.

Vcent_DQ(midpoint) is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DDR4 DRAM component. Each DQ pin Vref level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in figure 2.

JC-42.3C, Ballot 1727.84A
• Range from 45% of Vdd to 92.5% of Vdd
• Step size can be between 0.5%Vddq to 0.8%Vddq
  – Exact value will be specific to the DRAM and should be in the datasheet
Vref for Controller (Read)

- Single Vref for entire channel
  - Inexpensive, easy for controller to implement
  - Greater similarity required in DQ signal characteristics
Vref for Controller (Read)

- Single Vref for each DRAM in the rank
  - Allows for grouping of signals going to each DRAM
Vref for Controller (Read)

- Single Vref for each Lane in the rank
  - Allows for grouping of signals going to each Lane
  - Differs from previous setup only for x16 DRAMs
Vref for Controller (Read)

- Single vs. Multi-Rank support
  - Cost vs. layoutability
Generating the Eye

• Concept of Eye borrowed from SerDes
• No self-clocking, or clock recovery scheme
• Explicit clock or strobe at play
• In simulation run, cannot just specify frequency
  – Must incorporate clock/strobe
Eye - What the Strobe Sees

- Double Counted
- Not Counted
• Data running at 2400MT/s
• Clock P/N slightly offset to simulate poor trace design.
Compare Folding vs. Strobing

DQ Eye Sampled at Strobe

DQ Eye Wrapped at 416.67ps
Enabling DDR4 Simulation with Power Aware IBIS
I/O Modeling Options

- Simulating SSO is a desired part of system PDN design
- Choice of I/O model directly relates to simulation time and accuracy of SI and PI results
- Common choices include Spice, IBIS 4.2 and IBIS 5.0.
## Simulation Model Trade-offs

<table>
<thead>
<tr>
<th></th>
<th>SPICE Netlist</th>
<th>IBIS 4.2</th>
<th>IBIS 5.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation time</td>
<td>Longer</td>
<td>Shorter</td>
<td>Shorter</td>
</tr>
<tr>
<td>SI simulation accuracy</td>
<td>High</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>PI simulation accuracy</td>
<td>High</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>

### SSO Noise (Simulation)

- **SPICE Net**
- **IBIS 4.2**
- **IBIS 5.0 (HyperLynx)**

![SSO Noise Graph]

- **VDE**
IBIS Model Overclocking Concerns

- Traditional IBIS model algorithms assume max operating frequency related to length of V-T waveforms.
- “Length of a half cycle” ≥ “Length of Initial Delay” + “Length of Active Area”
- Initial Delay cannot be removed in IBIS 5.0 due to pre-driver switching currents.
Correcting Overclocking in the EDA Software

- Pre-driver and driver currents must be correctly summed relative to each switching event.
- Must support “Length of a half cycle” = “Length of Active Area”
Correcting Overclocking in the EDA Software

- Improved simulation algorithms generate correct results at every valid datarate.
System Level Simulation

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### ITEM | COMMENT
--- | ---
CHIP | 28nm Technology DDR4 Controller 32bit (4byte)
PKG | FCBGA 1444ball 31mm
PCB | Trough Hole Via 6 Layer
SDRAM | DDR4 SDRAM 16bit x 2 on Board (FLY-BY connection)

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<table>
<thead>
<tr>
<th>CHIP</th>
<th>PKG / PCB</th>
<th>SDRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>IO signal circuit</td>
<td>SPICE Net</td>
<td>S-parameter model (VSS reference)</td>
</tr>
<tr>
<td>IO power circuit</td>
<td>SPICE Net</td>
<td>IBIS5.0</td>
</tr>
<tr>
<td>SPICE Net Model</td>
<td>IBIS5.0 Buffer Model + RC Equivalent Circuit</td>
<td>IBIS5.0</td>
</tr>
<tr>
<td>IBIS5.0 Model</td>
<td>RC Equivalent Circuit</td>
<td></td>
</tr>
</tbody>
</table>
Simulation Schematic

- Includes Controller, x32 DQ bus, Address/Command
Simulation Results

- Single net simulation
- Excludes SSO and Crosstalk
- 2400 Mbps
- Comparison at SDRAM die pad
- Eye Widths (TdiVW) within 7ps (1.9%)

<table>
<thead>
<tr>
<th>SPICE Net Model</th>
<th>IBIS5.0 Model (HyperLynx)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EYE Width (min) = 361ps</td>
<td>EYE Width (min) = 354ps</td>
</tr>
</tbody>
</table>

![Simulation Results Diagram](image-url)
Simulation Results

- Simulation includes SSO noise
- 32 DQs and 4 DQ/DQS# pairs switching
- 2400 Mbps
- Comparison of VDE at controller die
- Comparison of DQ at SDRAM die pad
- SSO noise simulated accurately
Simulation Results

- Simulation includes SSO and Crosstalk
- 1 DQ as Victim net
- 31 DQs and 4 DQ/DQS# pairs as Aggressor nets
- 2400 Mbps

- Comparison at SDRAM die pad
- Eye Widths ($T_{diVW}$) within 22ps (7.3%)
- Some mismatch from un-modeled pre-driver delay sensitivity

![Comparison of SPICE Net Model and IBIS5.0 Model](image)
Conclusions

• EDA software is critical for DDR4 analysis
  – Use of DBI
  – Setting valid Vref levels
  – Rx masks for timing verification
  – Generate data eyes with correct jitter contributions

• IBIS 5.0 power aware models useful for system level analysis
  – Significantly speed up simulation time
  – Reasonable accuracy of SSO jitter effects
  – 60ns simulation duration (one cycle of PRBS7) – 98.6% sim time reduction!