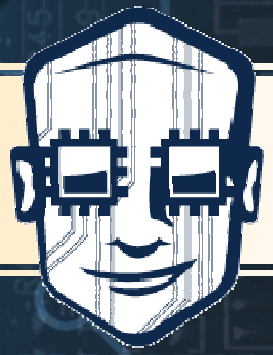
DesignCon® 2013
JANUARY 28-31, 2013
SANTA CLARA CONVENTION CENTER



Channel to Channel Crosstalk Behavior and Design Optimization for DDR4 Signaling

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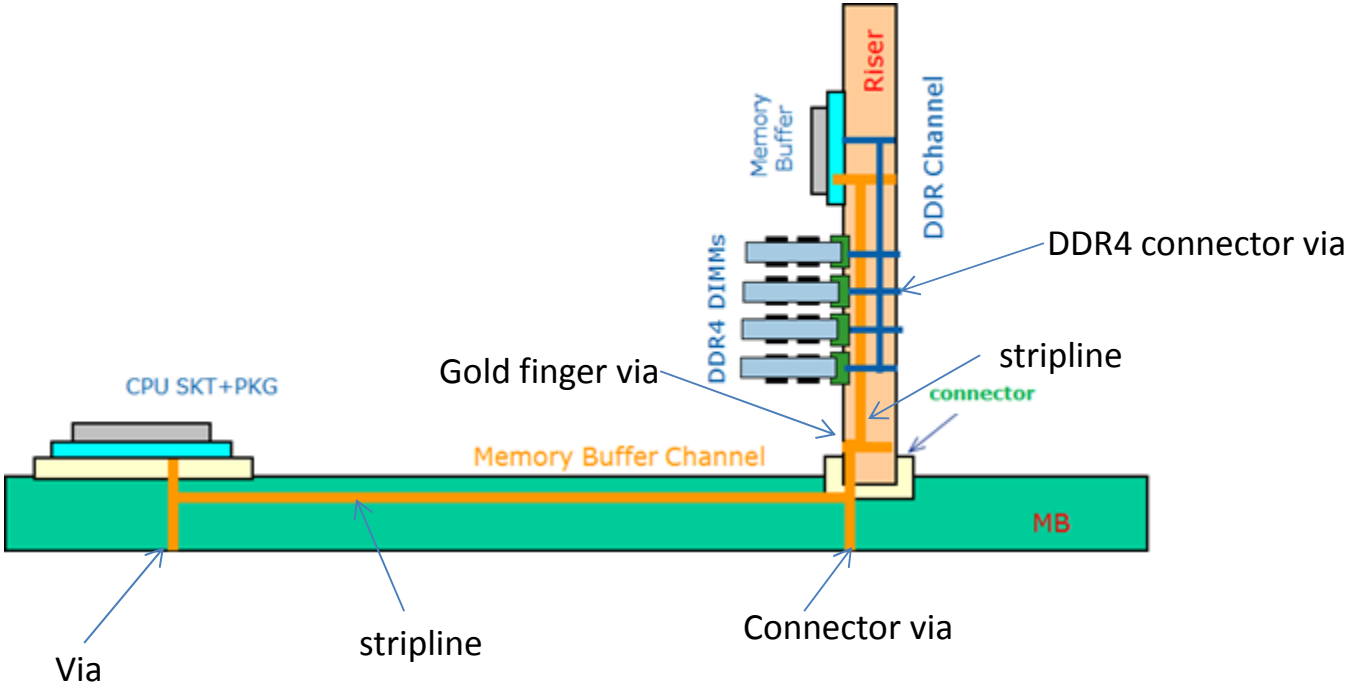
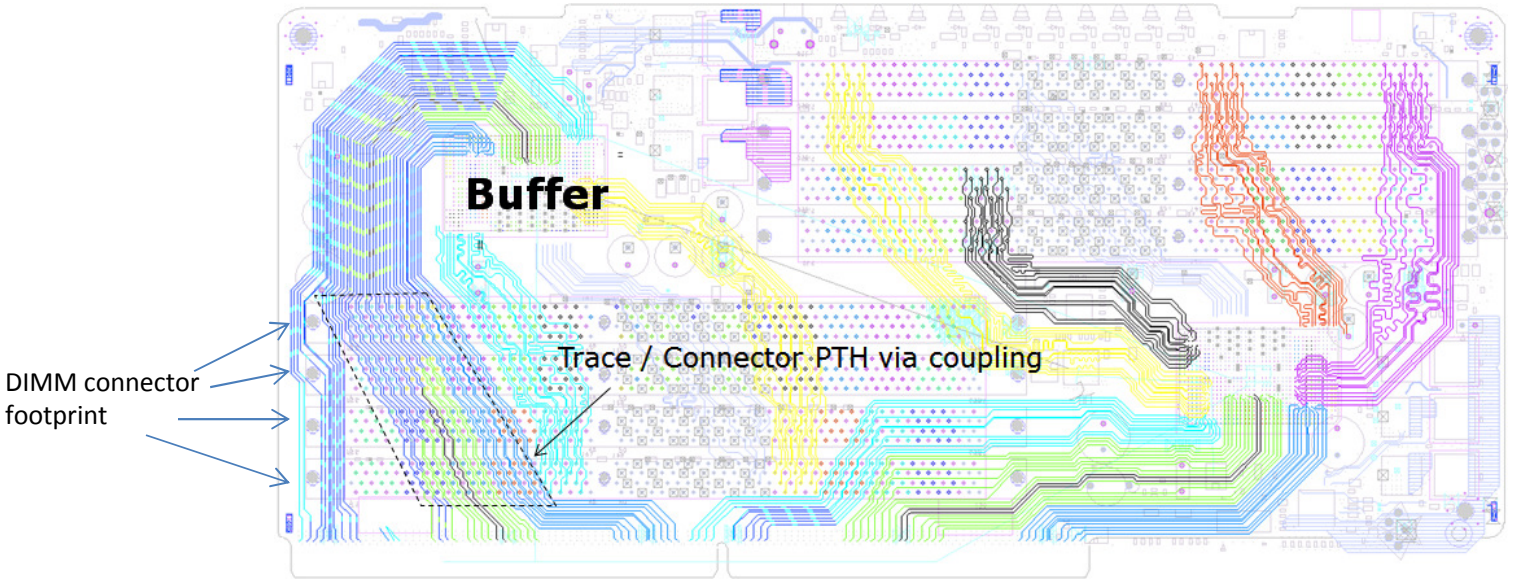
Introduction

- Memory buffer on riser card to increase memory performance.
  - high speed point to point topology
- DDR4 channels on the back side of the buffer



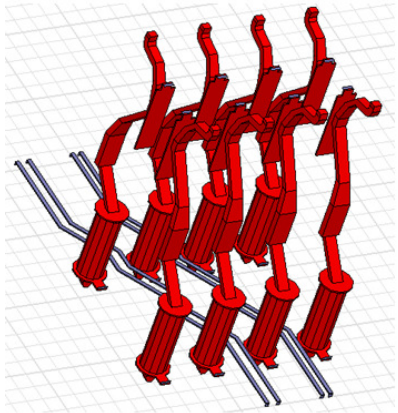
Buffer/DDR4 Coupling

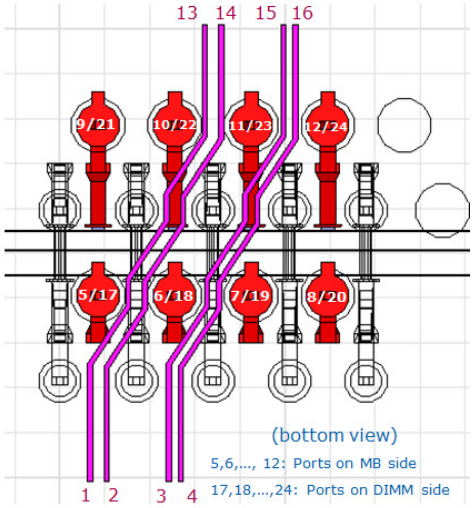
- Memory buffer channel routing through DDR4 connector field.
- DDR4 channel has coupling impact on memory buffer channel, while memory buffer channel has coupling impact on the DDR4 channel as well.

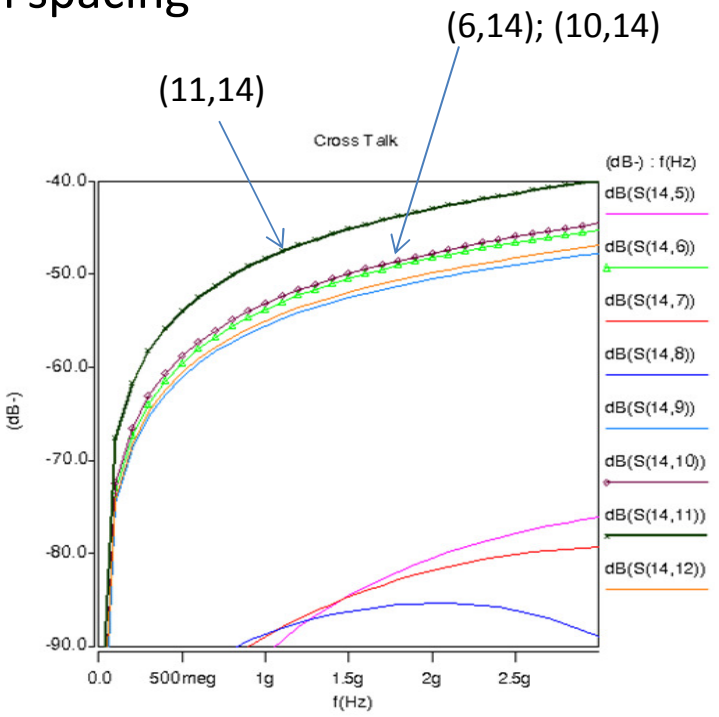


Buffer/DDR4 Coupling Model

- 3D model generated to include stripline trace from memory buffer channel and connector via from DDR4 backside channel
  - Line 1 and line 2 is 4.5mil width and 10mil spacing
  - Line 3 and line 4 are 4.5mil width and 6mil spacing

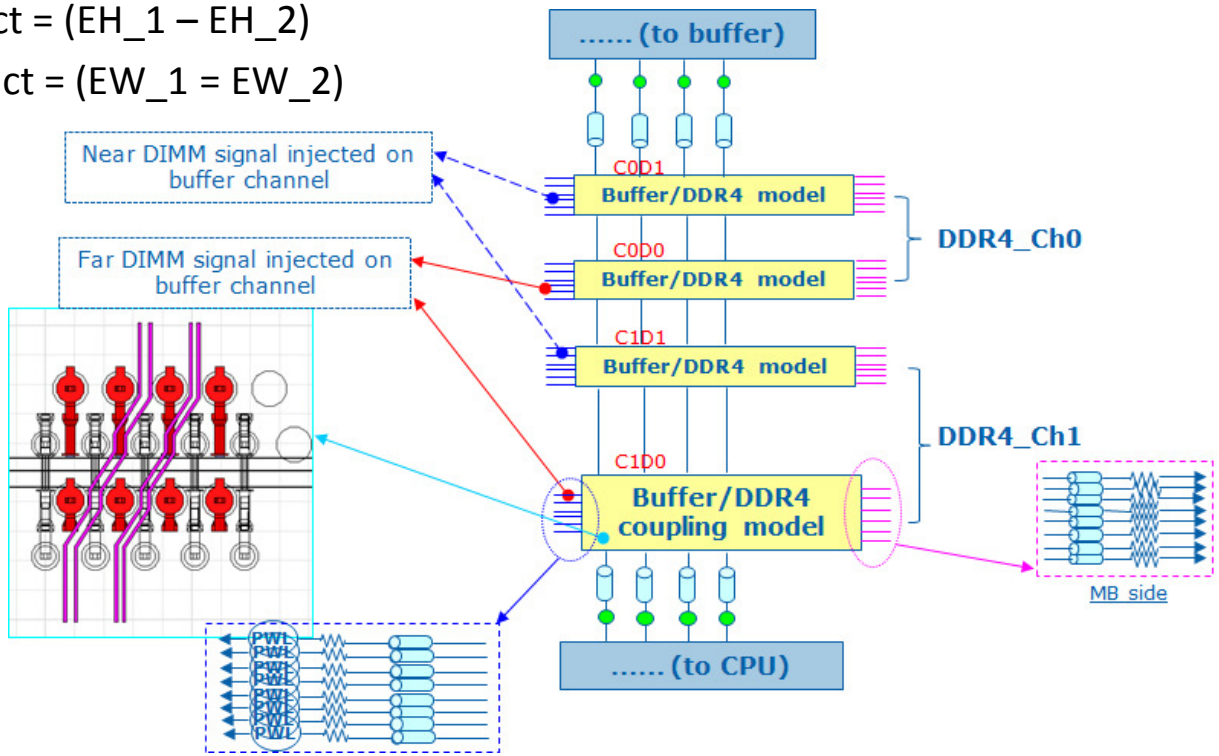






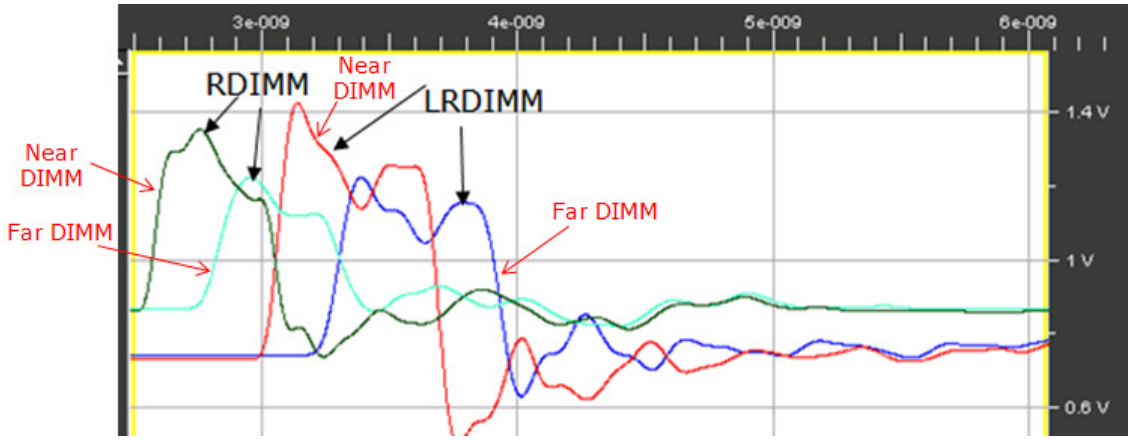
Time Domain Analysis

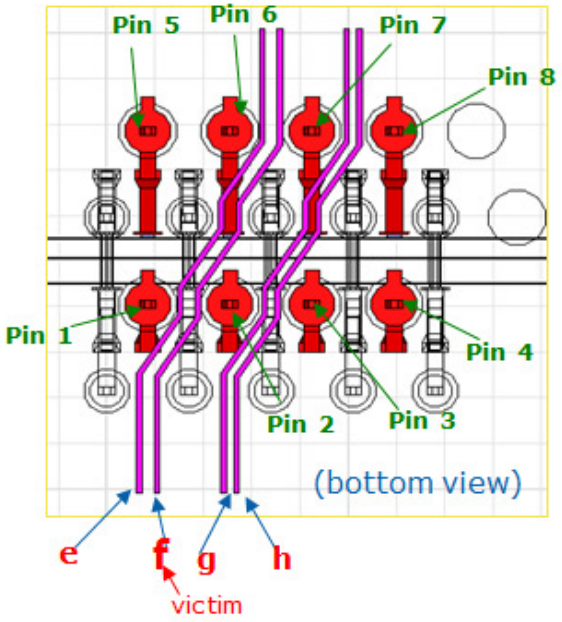
- Eye diagram of Memory buffer channel without DDR4 coupling
  - EH_1 and EW_2
- Eye diagram of memory buffer channel with DDR4 coupling
  - EH_2 and EW_2
- DDR4 coupling impact on buffer channel
  - EH impact = (EH_1 – EH_2)
  - EW impact = (EW_1 = EW_2)



DDR4 Channel Signaling

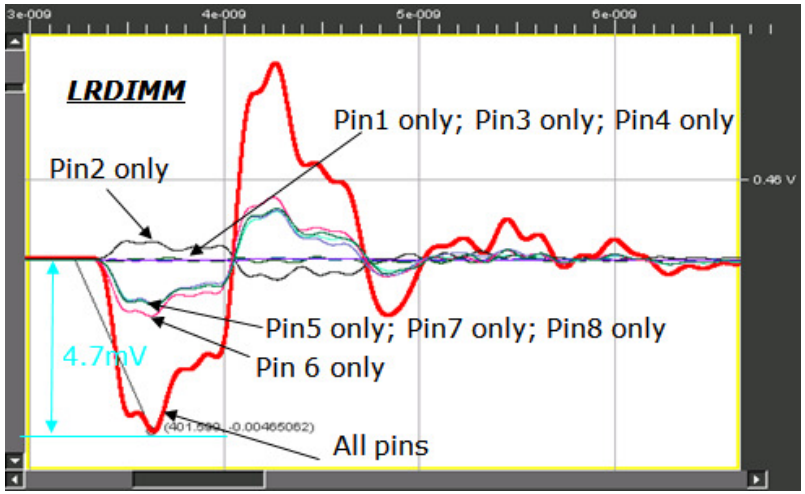
- 1.6GT/s with 2 channels and 2 DIMMs per channel (2DPC)
- DQ on DDR4 READ (Tx on DIMM side; Rx on Buffer side)
- Both RDIMM and LRDIMM checked
  - Waveforms saved as Piecewise Linear (PWL) voltage sources and injected on buffer channel through coupling model.

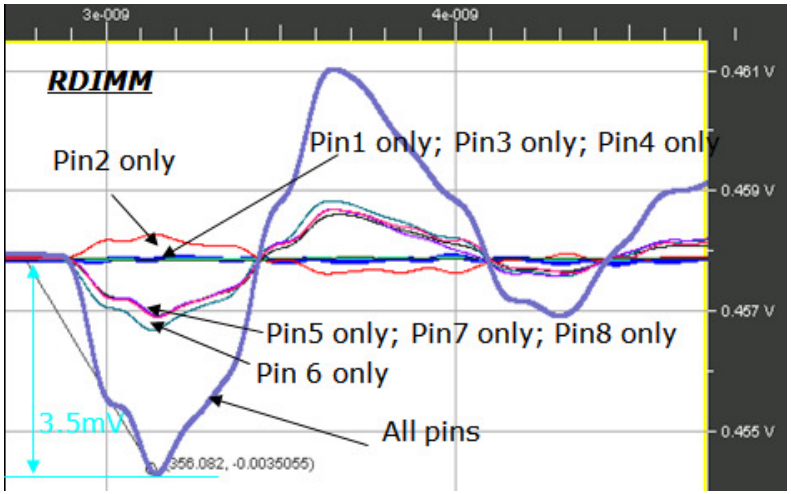




Waveforms on Buffer channel from DDR4 coupling

- Memory buffer channel Tx static
- DDR4 signals injected on memory buffer channel
- Waveforms measured on memory buffer channel Rx

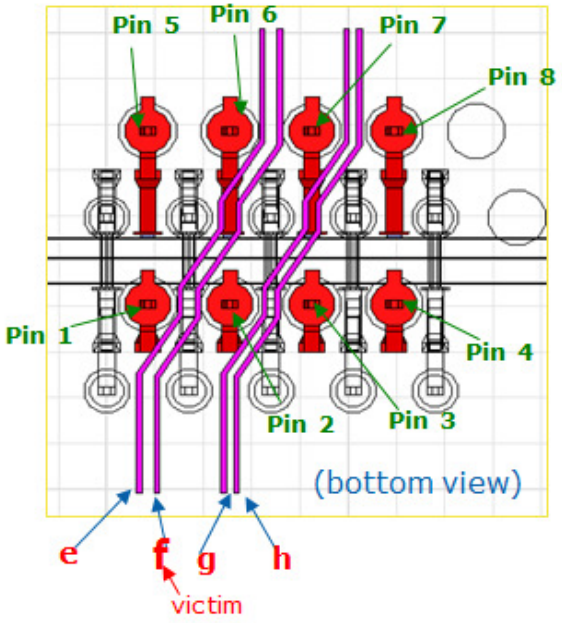




DDR4 Coupling on Buffer channel

- More impact from pin 5, 6,7,8
  - Single ground via row compared to pin 1,2,3,4 with two ground via rows

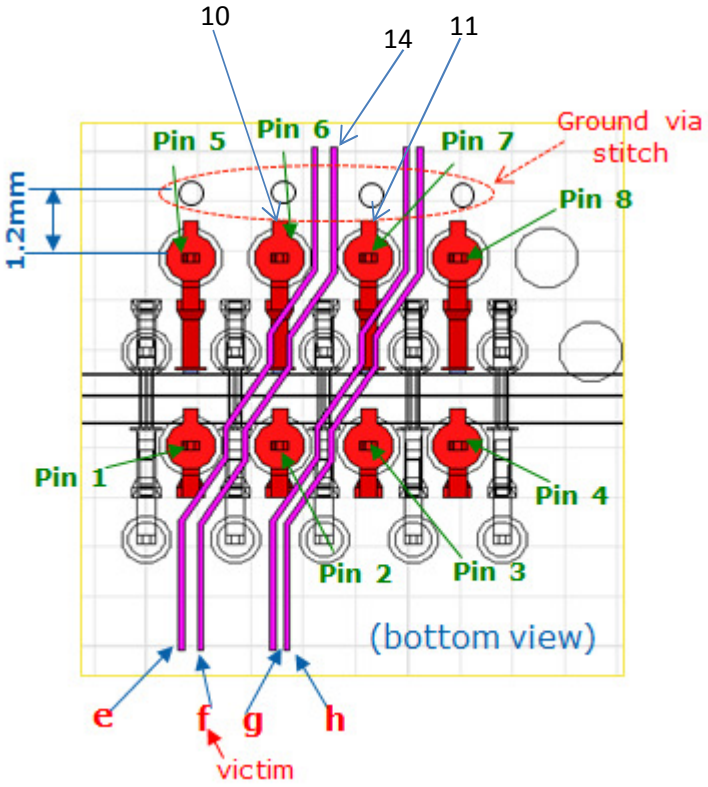
Item	Unit: EH(mV); EW(ps)	LRDIMM		UDIMM	
		ΔEH	ΔEW	ΔEH	ΔEW
a	DDR4 all pins Xtalk (8 Aggr.)	9.1	6.2	4.06	3.13
b	DDR4 Pin1 only	0.42		0.24	
c	DDR4 Pin2 only	0.99		0.43	
d	DDR4 Pin3 only	0.17		0.08	
e	DDR4 Pin4 only	0.05		0	
f	DDR4 Pin5 only	1.95		0.76	
g	DDR4 Pin6 only	2.46		1.09	
h	DDR4 Pin7 only	2.5		1.12	
i	DDR4 Pin8 only	2.14		0.90	
	Sum (Item b~i)	10.7		4.62	

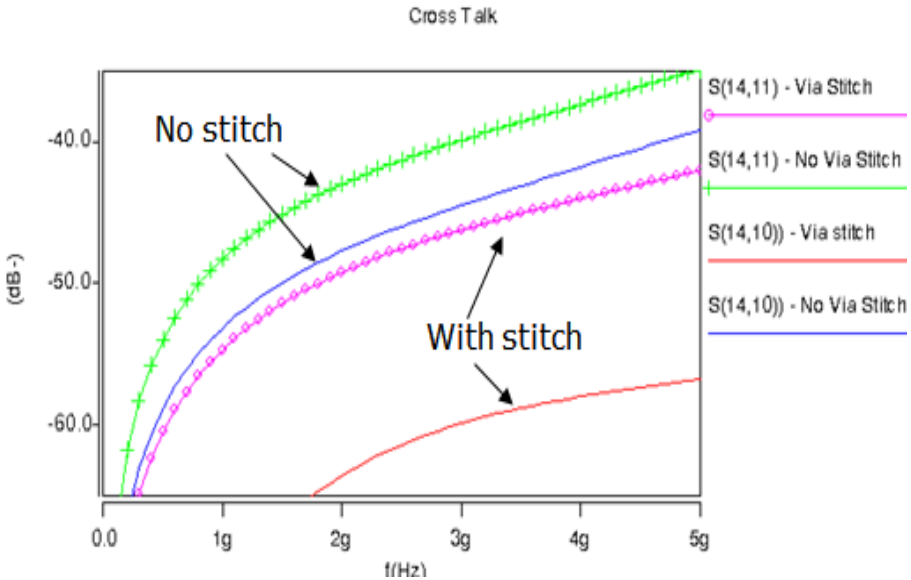


(Phase impact is not included)

Design Optimization

- Ground via (10-20-28) to reduce coupling





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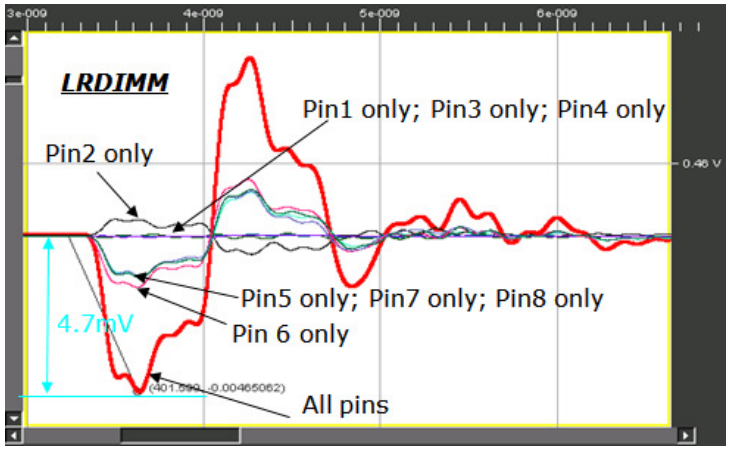
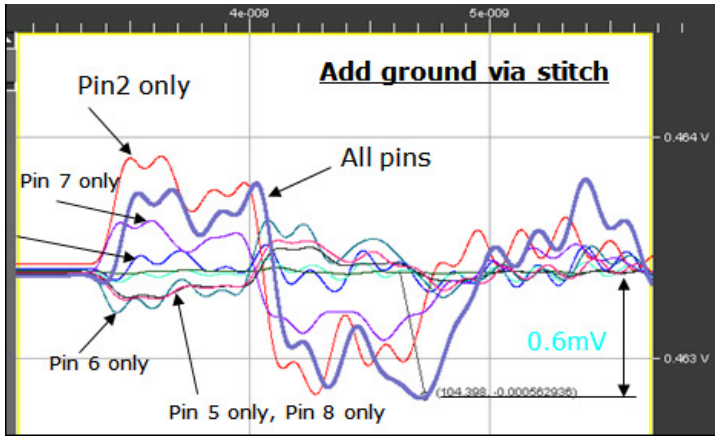


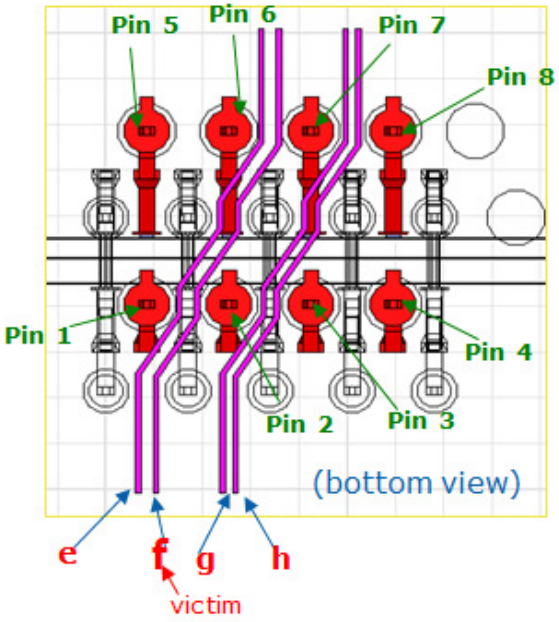


DDR4 Coupling on Buffer channel

- LRDIMM case:
  - EH impact reduced from 9.1mV to 1.8mV; EW impact can be ignored

Item	Unit: EH(mV); EW(ps)	LRDIMM		LRDIMM with Gnd via stitch	
		ΔEH	ΔEW	ΔEH	ΔEW
a	DDR4 all pins Xtalk (8 Aggr.)	9.1	6.2	1.8	0
b	DDR4 Pin1 only	0.42		0.43	
c	DDR4 Pin2 only	0.99		1.06	
d	DDR4 Pin3 only	0.17		0.16	
e	DDR4 Pin4 only	0.05		0.01	
f	DDR4 Pin5 only	1.95		0.13	
g	DDR4 Pin6 only	2.46		0.41	
h	DDR4 Pin7 only	2.5		0.67	
i	DDR4 Pin8 only	2.14		0.28	
	Sum (Item b~i)	10.7		3.15	

(Phase impact is not included)



Discussions

- The connector pinout used in the study is a combination of JEDEC DDR4 connector pinout patterns.
- Two track routing is assumed in the study. Much less impact is expected for single track routing
- DQ pins at the inner rows of DDR4 connector has less impact
- Implementation of ground via stitch may be limited due to system constraints, such as routing on other layers
- DDR4 system may support different topologies such as 3 DIMMs per channel (3DPC) at a relatively low speed, the impact is expected be similar or less.

DDR4 DIMM Connector Field Routing Recommendation

- Keep single trace routing if possible
- If two trace routing is needed, keep two-track routing through half of DIMM field and single track routing of the same trace though the rest DIMM field, thus to mitigate the coupling impact
- If two-track routing is needed, keep two-track routing for DQ pins located at inner rows of DDR4 RDIMM connector footprint
- If possible, add a ground via stitch near the DQ pins located at the outer rows of the connector footprint

Thanks