11-TP6: Power Integrity and Power Distribution Network Design

Power-Signal Co-Integrity Design for Multi-Gbps Low-Power DDR3 Mobile Platforms

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Agenda

- Background
- Silicon Modeling
- Channel Modeling & Verification
- Platform Analysis and Design
- Summary

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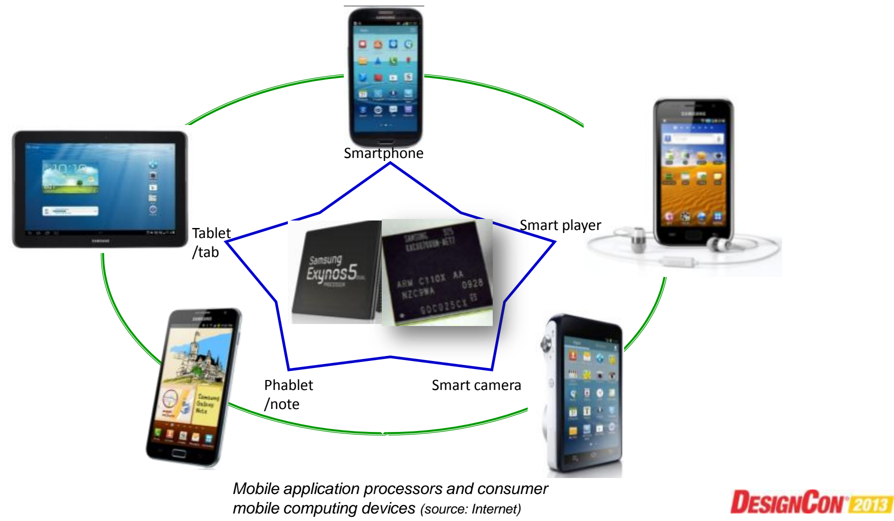
Background

- Consumer mobile computing devices are increasingly popular



Mobile application processors and consumer mobile computing devices (source: Internet)

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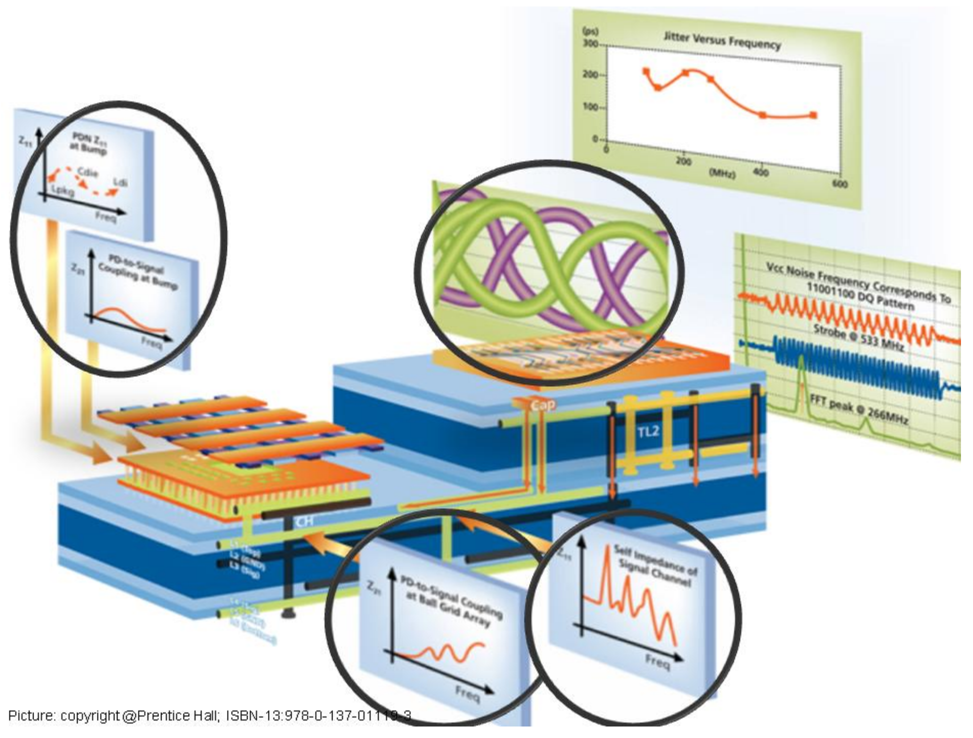

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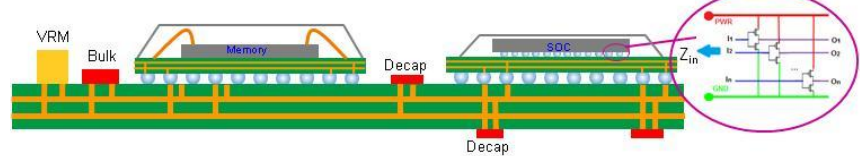
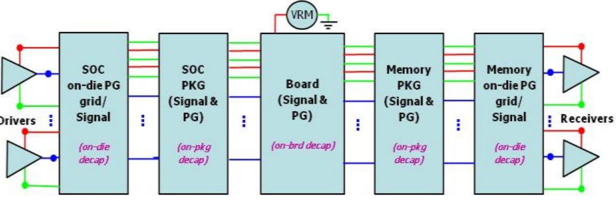
Mobile Memory Platform

- Processor chip communicates with LPDDR3 memory chip assembled on a printed circuit board



Typical high-speed & lower-power mobile memory platform

- In order to accurately characterize the platform, all components have to be considered

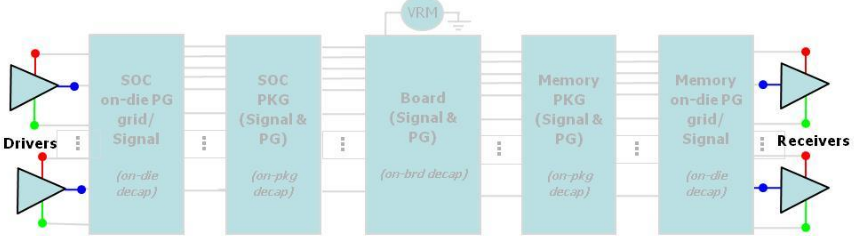


LPDDR3 mobile platform analysis block where data is written

Silicon Modeling

Macro Model for Output Buffer

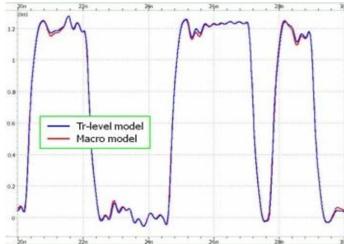
- In high-speed parallel data transmission, SSO noise is one of the concerns
- All output buffers sharing the same power domain have to be included for SSO simulation
  - A tr-level model for IO was used
    - ✓ High accuracy
    - ✓ Long simulation & high computer resources

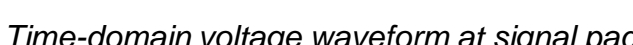


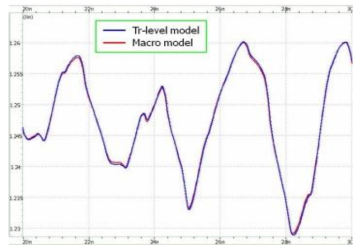
Silicon Modeling

Macro Model for Output Buffer

- An alternative method is to use behavioral macromodel
  - ✓ Extracted from Tr-level model
  - ✓ Achieve less simulation time & acceptable accuracy




Time-domain voltage waveform at signal pad

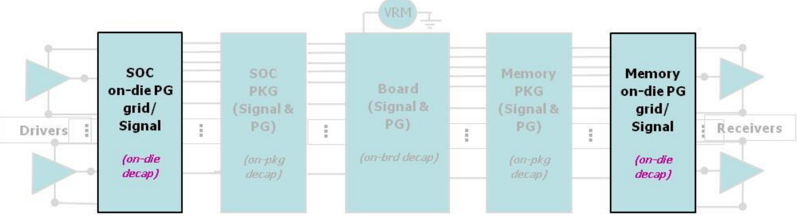


Time-domain voltage waveform at power pad

Silicon Modeling

On-Die P/G Modeling

- On-die P/G grid networks together with on-die decaps become the impact
- The shortcoming of the previous models & methodologies
- Two analysis approaches are used, depending on data availability
  - Method I: Model extraction based the detailed RC model *(for memory chip)*
  - Method II: The model extraction from design (*for SOC chip*)

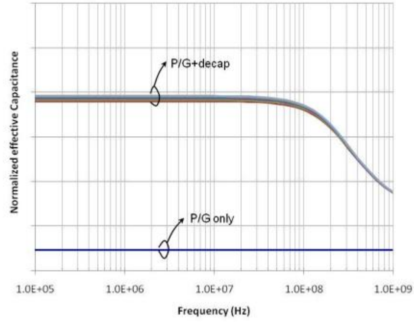


Silicon Modeling

On-Die P/G Modeling

Method I: Compact model extraction from the detailed RC model

- The detailed RC model is available, however
  - Too large to be suitable for channel analysis
  - A typical model with the size of ~100MB and 0.5M MOS transistors
  - Compact model is feasible to speeds up channel simulation
- On-die P/G grid behavior together with on-die decap



Effective input capacitance of P/G grid with & without on-die decap

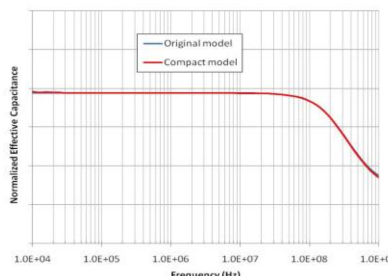
- Its variation is small, less than 4% when power supply changes from 0.9V to 1.5V.
- On-die P/G grid has significant capacitive parasitics
- It is approximately voltage-independent
- It is freq-dependent due to RC parasitics

Silicon Modeling

On-Die P/G Modeling

- The extraction of compact model
  - the assumptions
    - ✓ Linear small signal
    - ✓ Nominal voltage applied in the frequency range of interest.
  - Model extraction flow

  - Accuracy verification
    - ✓ Through effective input capacitance in frequency domain



Effective P/G grid's input capacitance

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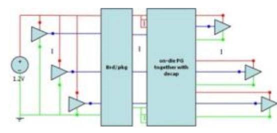
Silicon Modeling

On-Die P/G Modeling

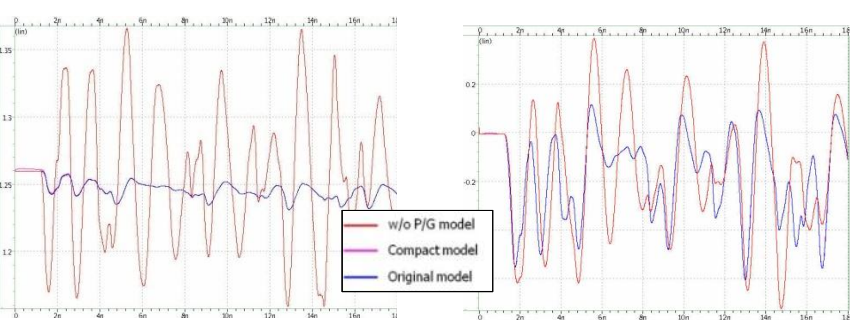
- Time-domain verification

  Three cases are considered
  - (a) Original P/G model
  - (b) Compact model
  - (c) Removal of P/G grid (used for checking how large impact of P/G grid)



Schematics used for TD verification

Conclusions:
- **High accuracy**
- **4x speedup in simulation**



Voltage at receiver's power supply pads

Current through power supply source

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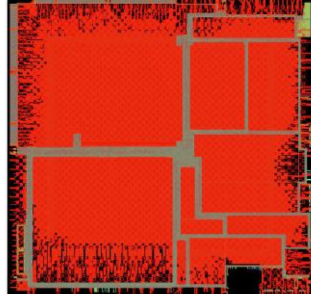
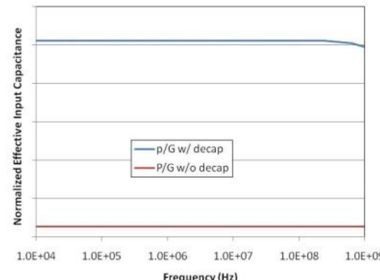
Silicon Modeling

On-Die P/G Modeling

Method II: P/G model extraction from chip design
- Chip design with def/lef or GDSII is used
- A SPICE-compatible P/G grid model can be extracted
  - Commercial tool is used
  - Include the decap designed in pad cells
  - Remain the dependence of decap's location
- Case show



Chip design used for P/G model extraction



Effective input capacitance of one P/G grid extracted from a chip design

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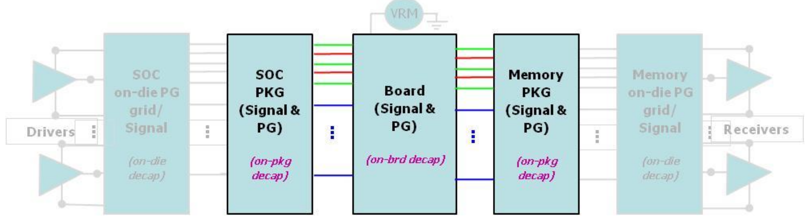
Channel Modeling & Verification

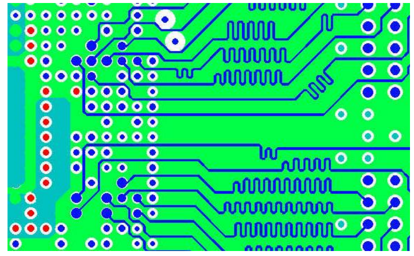


- Combined Power/Signal Analysis
- PDN Analysis and Design
- Signal Analysis and Design

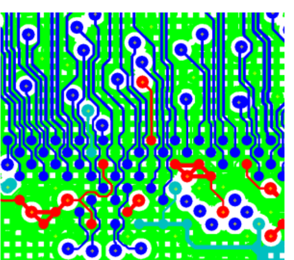
Channel Modeling & Verification

Separated vs Combined Modeling

- Signal paths in package & board are coupled with PDN system



Signal & PDN layout in two intermediate layers at one PCB design showing weak coupling between power and signal paths



Signal & PDN layout in top two layers at one package design showing strong coupling between power and signal paths

Red: power
Green: ground
Blue: signal

- The models are extracted through electromagnetic simulation to capture all dominant EM effects
- Two methodologies were used:
  - PDN is simulated separately from signal paths to speed up the modeling
  - Signal paths are simulated together with PDN to capture their coupling

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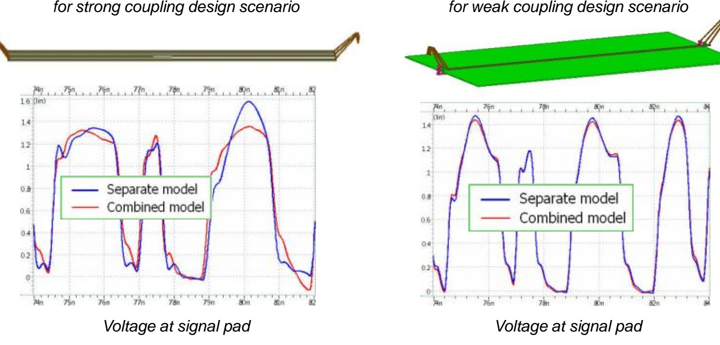
Channel Modeling & Verification

Separated vs Combined Modeling

- Demonstrate both the methods with the simplified cases



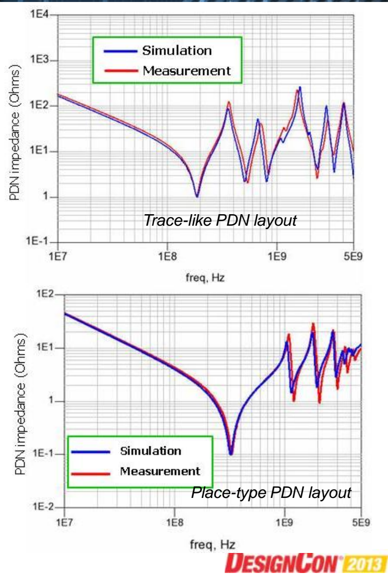
- Observation: Significantly different results for strong coupling scenario
- Conclusions
  - The separate model can be safely used at initial design/optimization stages if only weak coupling exists to achieve the efficiency
  - At final verification, the combined PSI model needs replace it to achieve high verification accuracy.

Channel Modeling & Verification

Bare Channel PDN Design

- PDN becomes one of the dominant performance limiting factors
  - Needs instantly supply enough transient currents whenever IO buffers need
  - Acts as shielding
  - Use as current return path for high-speed signals
- It is necessary to fully analyze electromagnetic effects
- PDN network is designed hierarchically
- PDN design
  - Power nets are sandwiched by ground planes
  - Power nets should be routed as plane and completely sandwiched by ground planes
  - Multiple power vias are inserted as close to ground vias as possible
  - Trace-like layout should be avoided

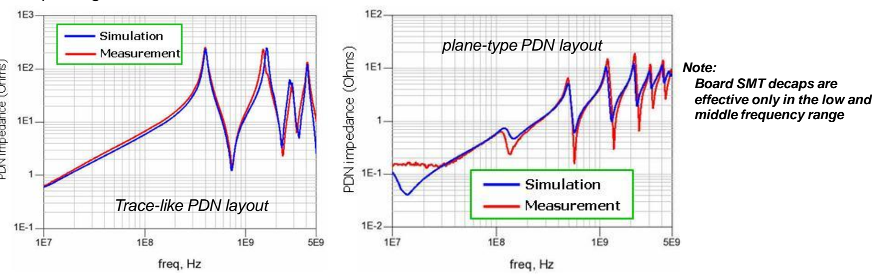
    Has the impedance one order higher than plane-type one



Channel Modeling & Verification

Channel Decap Design

- Decap design



Note:
Board SMT decaps are effective only in the low and middle frequency range

Self impedance of two PDNs with different PCB layouts with the decaps

- Self impedance of PDN consisting of board, package and chip seen from PCB side (including on-board/on-die decap)
  - Simulation results w/ & w/o the effect of on-die P/G grid are included
  - The extracted P/G model is indirectly verified
  - The correlation is quite good

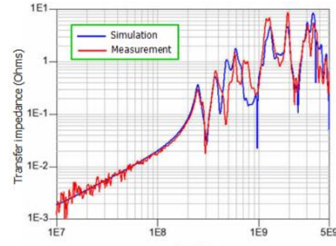
PDN's Input impedance profile including the effects from PCB/pkg/chip

Channel Modeling & Verification

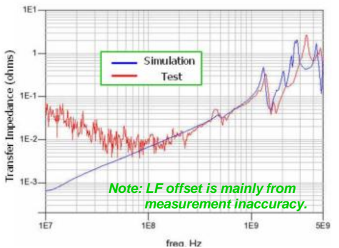
PDN Coupling

- Noise coupling between PDN system
  - A determining factor in some design
  - Transfer impedance indicates that HF noise is more easily coupled each other
- Two ways in noise coupling from PDN to signal
  - Power rail's fluctuation changes power supply to IO buffers, which translates into signal noise
    - ✓ Solution
      - Stable power supply through well-design PDN with good decoupling solution
      - Transmitter insensitive to power fluctuation
  - PDN noise is coupled into signal path through channel coupling
    - ✓ Transfer impedance is a good indicator
- Conclusion

  The combined modeling is necessary at LPDDR3 & beyond



Transfer impedance from one PDN to the other



Far-end power-to-signal transfer impedance

Channel Modeling & Verification

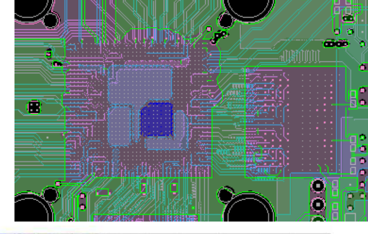
Signal Design

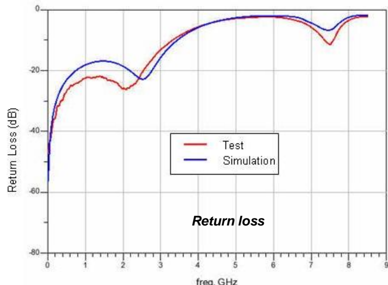
- Signal design
  - Impedance control for transmission line
  - Signal path transition design
  - Signal isolation
- Signal via is more capacitive
  - Via structure is largely determined by fabrication process
  - Parameters used for via optimization
    - Pad/antipad size
    - Via number
    - Via spacing with power/ground vias
  - Stacking via has better performance than staggered one, but higher cost
  - Plating through hole
    - Pad removal in intermediate layers is desirable for capacitive reduction
    - Long stub has negative impact
- Bonding wire is inductive
  - Bonding wire design
    - Minimize its length
    - Lower wire profile
    - Routes it together with P/G bonding wires

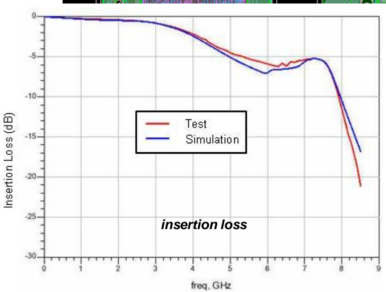
Channel Modeling & Verification

Signal FD Verification

- DQ signal path in LPDDR3 memory channel in PCB board
  - Return loss & insertion loss data are provided through test and simulation up to 9GHz
  - Good performance up to 4GHz for LPDDR3 operation







Return loss and insertion loss of a designed single-ended signal path

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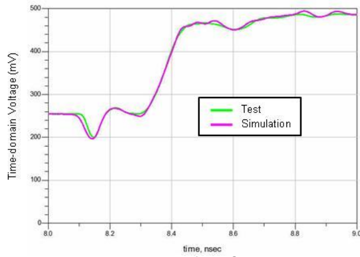
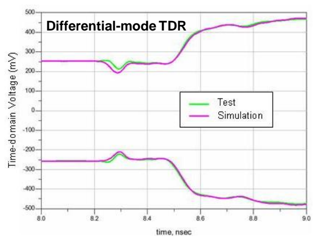
Channel Modeling & Verification

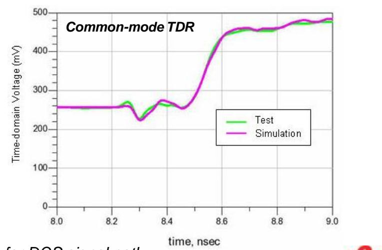
Signal TD Verification

- DQ signal path in LPDDR3 memory channel in PCB board
  - A dip after the signal is injected is cause by capacitive PTH via
  - The simulation is correlated well with the test
- DQS signal path in LPDDR3 memory channel in PCB board
  - Differential-mode vs common-mode TDRs
  - The dips are caused by capacitive PTH via
  - Simulation and measurement data are correlated well



TDR signature for DQ signal path





TDR signature for DQS signal path

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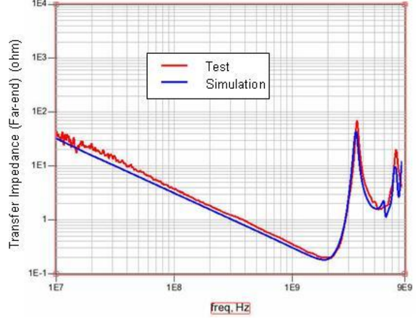
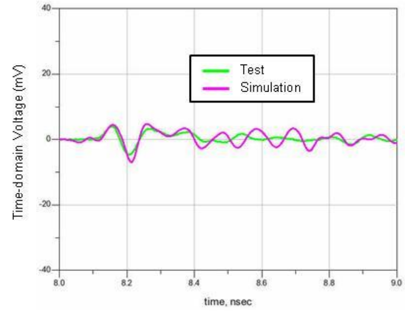
Channel Modeling & Verification

Signal Coupling

- The coupling in DQ signal paths in LPDDR3 memory channel at board
  - ✓ Transfer impedance for far-end crosstalk
  - ✓ TDT curve test for far-end crosstalk
- Weak coupling due to strip form



Far-end crosstalk in frequency domain



Far-end crosstalk in time domain

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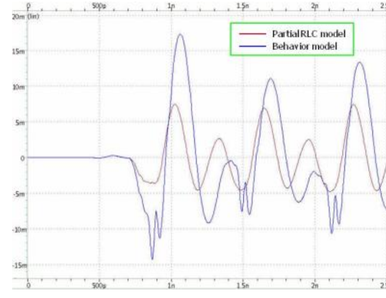
Channel Modeling & Verification

Global Grounding

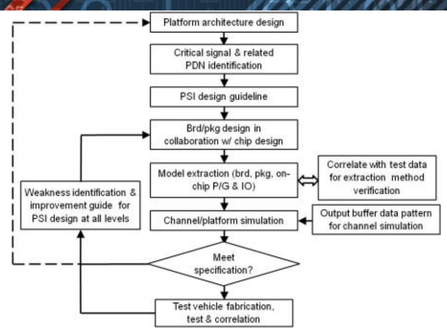
- IO buffers at both sides of channel have global ground node
  - A sneaking path is formed
- If partial RLC-based model is used in channel simulation, the sneaking path by-passes its non-ideal ground
- It is necessary to have common ground reference for the models
  - Solution: new behavioral models with common reference node
  - Case demonstration
    - ✓ Partial RLC model only for chip's redistribution layer as case study
    - ✓ By-passing effect underestimates the noise



Time-domain voltage waveform on signal pad of a receiver

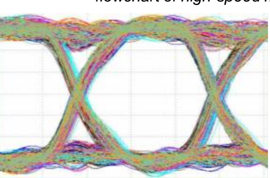
Platform Analysis and Design

- Channel analysis and design chart
  - ✓ Use design guidelines for initial design
  - ✓ Need collaborations from multiple parties
  - ✓ Methodology verification is critical
  - ✓ Keep the followings in mind during design
    - Routability
    - Cost for design improvement
    - Design/redesign time
    - Impacts of design improvement to others
    - Need trade-off
    - Final verification



flowchart of high-speed mobile channel analysis and design

- Mobile LPDDR3 channel
  - ✓ Eye-diagram is shown left
  - ✓ The correlation is future work



Eye diagram of one byte in LPDDR3 mobile channel simulation

Summary

- An efficient & accurate silicon modeling method has been demonstrated for PSI combined analysis.
- Channel simulation models have been verified over 5GHz and the power/signal co-modeling was necessary for mobile platform design beyond 1GHz.
- Combined power-signal integrity co-analysis and design flow has been demonstrated and verified with frequency- & time-domain correlations.
- The combined method was able to predict PSI-related issues more precisely and pinpointed potential issues at the early design stage.
- Eye measurement and simulation correlation is being progressed and the proposed methodology/flow can be applied for LP DDR3 extension and LP DDR4 platforms.

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Thank you

Q&A