EMC種子課程

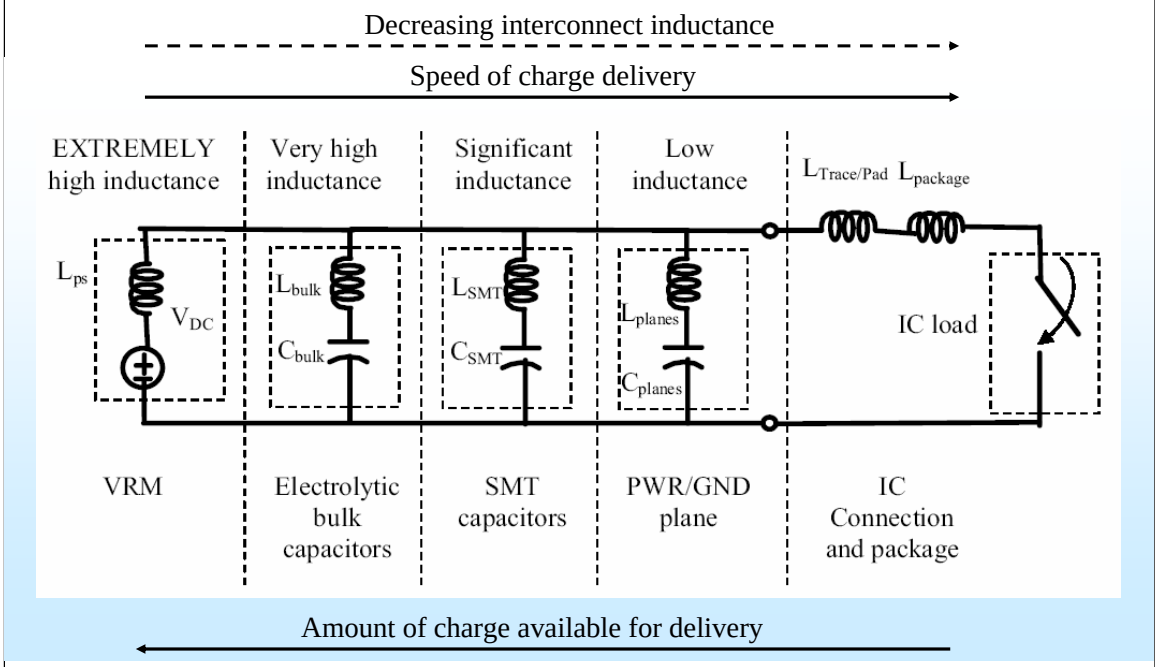
Lesson 3

陶瓷(Ceramic)去耦合電容值的選擇

論文出處與簡介

- http://www.ieee.org/organizations/pubs/newsletters/emcs/fall05/practical.pdf
  - IEEE EMC Society Newsletter, Issue No. 207, Fall 2005, pp. 46-53.
- 本論文內容
  - 電源網路系統(PDN)各頻帶的供電模型
  - 電源網路系統各頻帶的去耦合電容成份
    - 寄生電感影響去耦合電容的速度以及工作頻帶
  - 決定全頻帶去耦合電容值的兩種設計方式
    - 訊號完整性(SI)領域常用的方法
    - 電磁干擾(EMI)領域常用的方法

THE POWER BUS FUNCTION



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-- A PDN (power distribution networks) is comprised of several elements, including the VRM module (Voltage Regulator Module, i.e., dc/dc converter), bulk capacitors, SMT decoupling capacitors, and power/ground plane pairs (power bus).

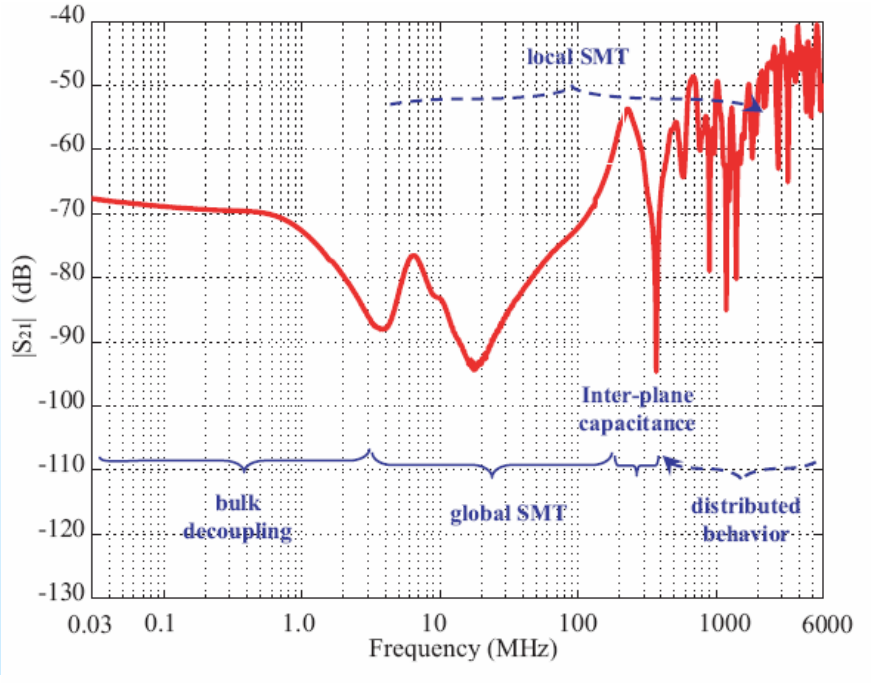
-- The effectiveness of each element in delivering sufficient charge with adequate speed is not uniform, because the parasitic inductance impedes changes in the current.

-- A charging hierarchy exists based on the rate of charge delivery (usually impeded by distance and inductance) and charge storage capacity

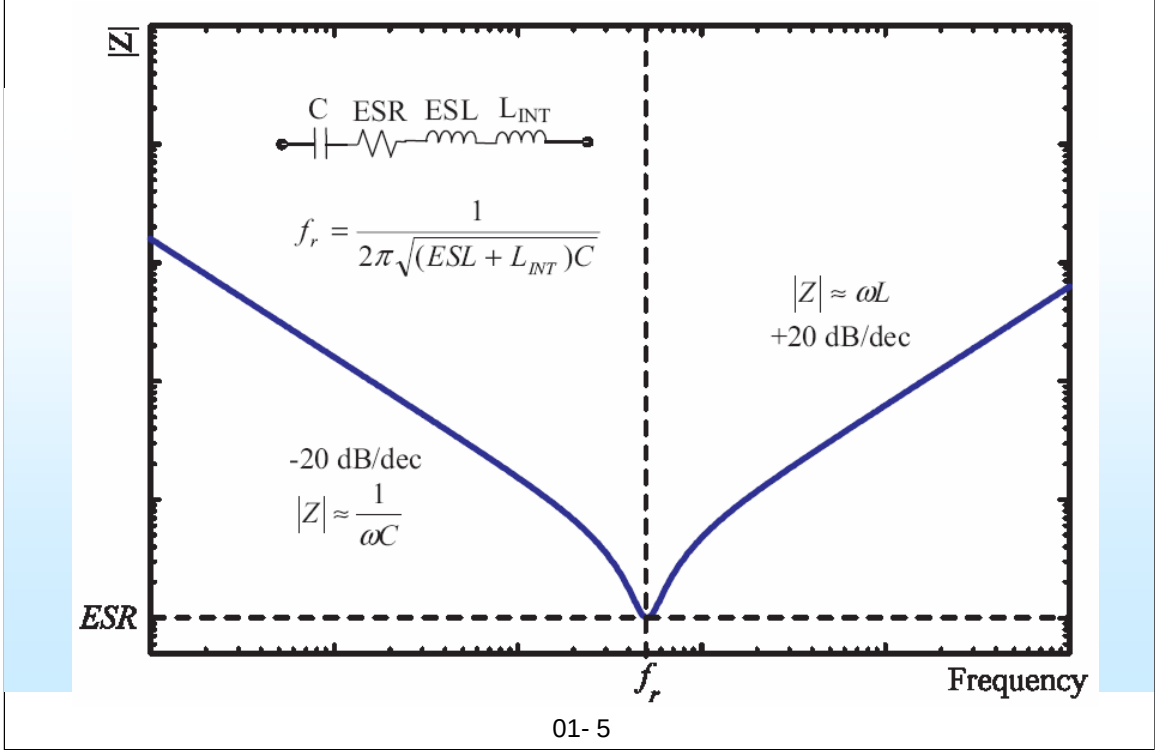
-- The VRM and the bulk capacitors are usually few in number and are located in specific areas of the PDN due to their dimensions and other constraints. High-frequency decoupling capacitors are usually large in number and are typically easily located

with a greater flexibility.

THE DECOUPLING CAPACITOR



Interconnect Inductance



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-- The parasitic inductance consists of an inductance associated with the capacitor itself (equivalent series inductance, or ESL) and inductance associated with the means of connecting the capacitor between power and ground planes (the solder pads used to secure the capacitor to the PCB and any traces and/or vias used to make the electrical connections).

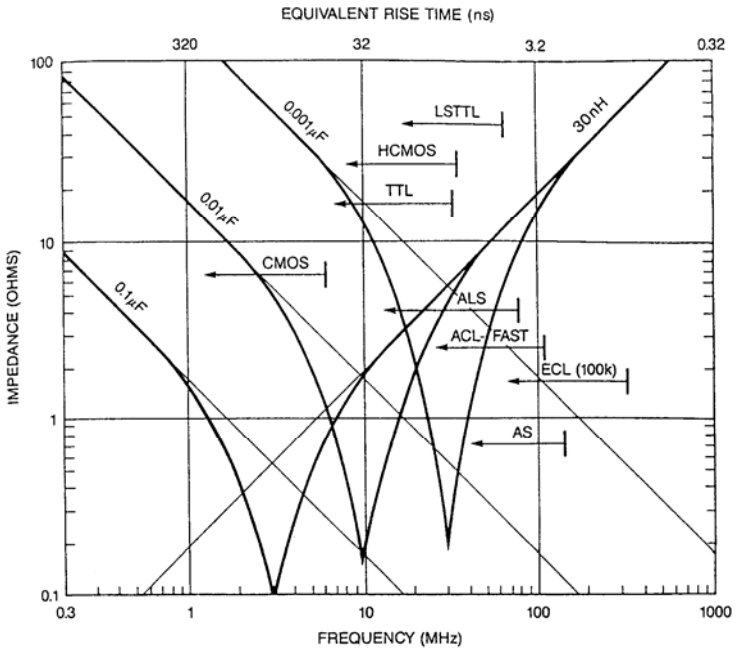
-- At frequencies higher than this resonant frequency, the capacitor behaves inductively and is ineffective in decoupling.

-- If the resonant frequency is shifted higher in frequency by lowering the parasitic inductance, decoupling can be made more effective at higher frequencies. (so design very short traces and low-inductance pad land to get min. parasitic inductance on PDN)

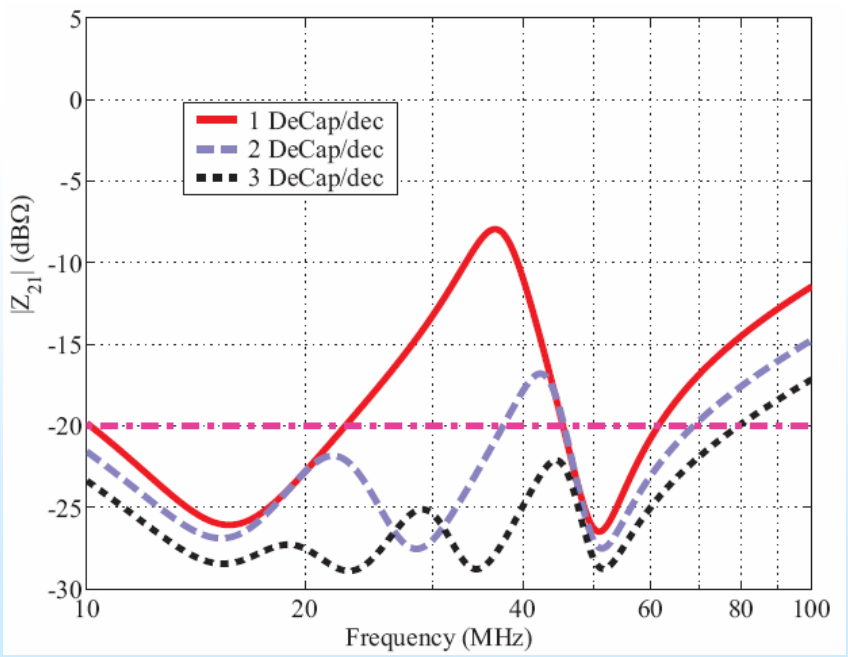
-- the multilayer configuration of the ceramic capacitors (MLC) allows controlling the values of the equivalent series inductance by adjusting the height, width, length and number of pad connections, accordingly

-- Several fabrication technologies are available for ceramic capacitors, i.e., the reverse geometry or low inductance chip capacitor (LLIC) configurations, where the current flows into the decoupling capacitor from the wide sides, the inter-digitated configuration (IDC), where multiple connections are employed, and the low inductance chip array (LICA) configuration, where the decoupling capacitor is mounted as a flipchip component

Determining Individual Decoupling Capacitor Values
Approach A: The SI community



Determining Individual Decoupling Capacitor Values Approach A: The SI community



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-- This approach uses an **array of values** of decoupling capacitors. **Uses three capacitor values per decade** to achieve the flattest PDN impedance vs. frequency profile to maintain an upper bound “target impedance”

-- The **three** capacitor values are typically chosen so that they are **logarithmically spaced** (i.e. 10, 22, 47, 100 nF,etc). The use of **two** capacitor values (i.e. 10, 33, 100 nF, etc) or a **single** capacitor value (i.e. 10, 100, 1000 nF, etc) per decade can be employed but does not usually provide a PDN impedance profile that is sufficiently flat. (在每10倍的頻帶寬內,並用對數倍率的三值陶瓷電容,壓低全頻帶)

-- The effectiveness of this approach is somewhat dependant on the value of ESR of the capacitors and the resulting series/parallel resonant frequencies of the decoupling capacitors to maintain the impedance to be below the desired target impedance over the frequency range of interest.

Determining Individual Decoupling Capacitor Values
Approach B: The EMI community

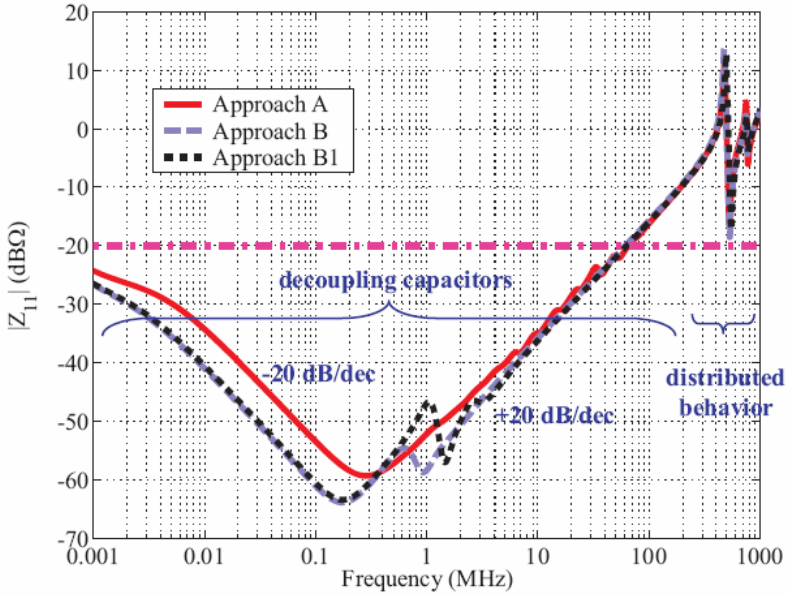

Figure 8: The driving point impedance, Z_{11}, of a power bus showing a comparison of design Approaches A and B for choos-

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-- A prominent view in the EMI community for PDN design for high-speed digital PCBs is that the specific values of decoupling capacitors need not be as carefully chosen as in the previous approach.

-- Approach B, addresses the high-frequency ceramic decoupling specifically and **employs the largest value** of capacitance available in the specific surface mount technology (SMT) package size to yield a PDN impedance profile that is acceptably flat. (用該封裝中最大value的SMD陶瓷電容硬把全頻帶衰減)

-- At low frequencies, Approaches B and B1 provide a lower impedance, which is a manifestation of the higher capacitance used.

-- In these examples, it is clear that either approach can achieve the design goal on PDN transfer impedance and have nearly identical performance above frequencies of a few hundred MHz. **Use of a single value** of capacitance **in the largest value in the package size** may provide the benefit of simplicity of design and manufacture. (這是因爲很多的SMD電容並聯效果,已經把單顆C所看到的寄生電感效應自然打折了,所以同封裝size中取vlaue大者爲佳)

-- Changing the design parameters (PCB characteristics, power bus characteristics, capacitor characteristics, etc.) will alter the impedance curves regardless of the design approach used, but will not change the overall conclusion that there is little difference in the PDN impedance profiles between

Approaches A and B (and B1).

Determining Individual Decoupling Capacitor Values
Approach B: The EMI community

Capacitor Description					# of Caps		
Value (nF)	ESR (mΩ)	ESL (nH)	Inter-connect (nH)	Type	A	B	B1
3.30E+06	60	15	2	E-lytic	1	1	1
100000	11	1.4	2	1812	4	16	16
47000	12	1.4	2	1812	4		
22000	14	1.4	2	1812	4		
10000	16	1.4	2	1812	4		
4700	16	0.5	1.6	0603	4	24	
2200	19	0.5	1.6	0603	4		
1000	23	0.5	1.6	0603	4		
470	29	0.5	1.6	0603	4		
220	23	0.5	1.6	0603	4		
100	30	0.5	1.6	0603	4		
47	40	0.4	1.35	0402	4	20	44
22	55	0.4	1.35	0402	4		
10	75	0.4	1.35	0402	4		
4.7	104	0.4	1.35	0402	4		
2.2	211	0.4	1.35	0402	4		
Total # of Decoupling Capacitors =					61	61	61
Total Capacitance (milliF) =					4.05	5.01	4.90

-- For the same number of high-frequency ceramic decoupling capacitors, more total capacitance is often achieved in Approach B than with Approach A.

-- The PDN dimensions correspond to a PCB that is 6 in. x 9 in. with a single power/ground plane pair power bus of thickness 10 mils. The PCB material is chosen to exhibit a dielectric constant of 4.5, and a loss tangent of 0.02; a relative permeability of unity; and a plane capacitance of 2.426 nF.