EMC種子課程

Lesson 1

電源去耦合電容最佳擺放方式

Outlines

- 參考論文出處與簡介
- 何種情況下，去耦電容的位置有影響
- IC旁的電源去耦合電容模型
- 寄生電感對去耦合電容的影響
- 多層板IC旁的電源去耦合電容模型
- 降低電源去耦合電容的方法
- 兩層板電源去耦合電容最佳擺法

參考論文出處與簡介

- http://www.ieee.org/organizations/pubs/newsletters/emcs/winter06/practical_1.pdf
  - IEEE EMC Society Newsletter, Issue No. 208, Winter 2006, pp. 56-67.
- 本論文內容
  - 何種情況下，去耦電容的位置會有影響?
  - 以時域、頻域的角度分析說明

何種情況下，擺放電容的位置有影響

- 去耦合電容作用全域有效，或是與其擺放位置相關?
  - 與電容本身無關，而是與電容所存在的環境有關
- 兩個評估去耦合電容作用是否與位置有關的指標
  - 若IC可得的電流與電容位置有關
  - 若電源電壓與電容位置有關

IC旁的電源去耦合電容模型

- 去耦合電容引入的寄生電感ESL與ESR，是影響電容充放電效果的主要因素
  - 去耦合電容越靠近IC，效果越好
  - $L_{TOTAL} = L_{above} + L_{below}$

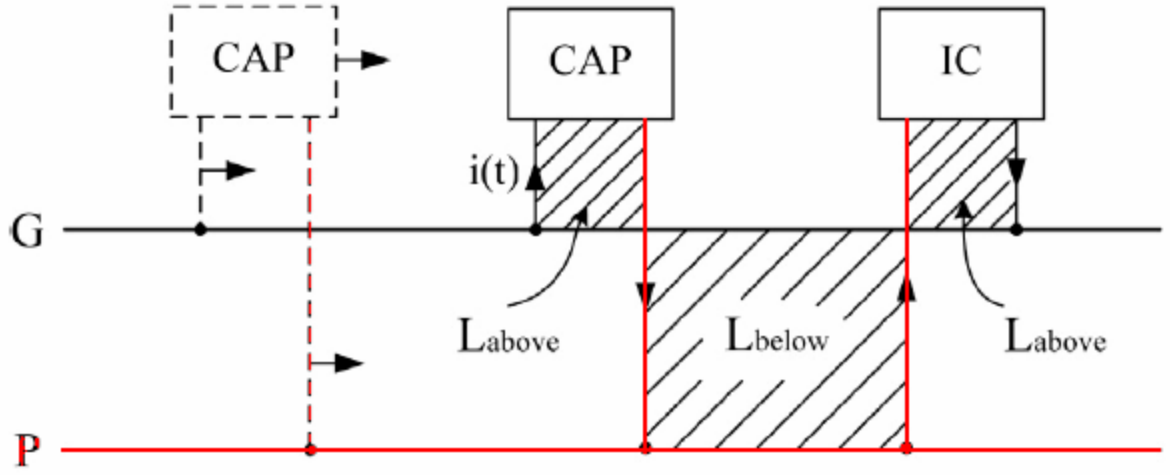
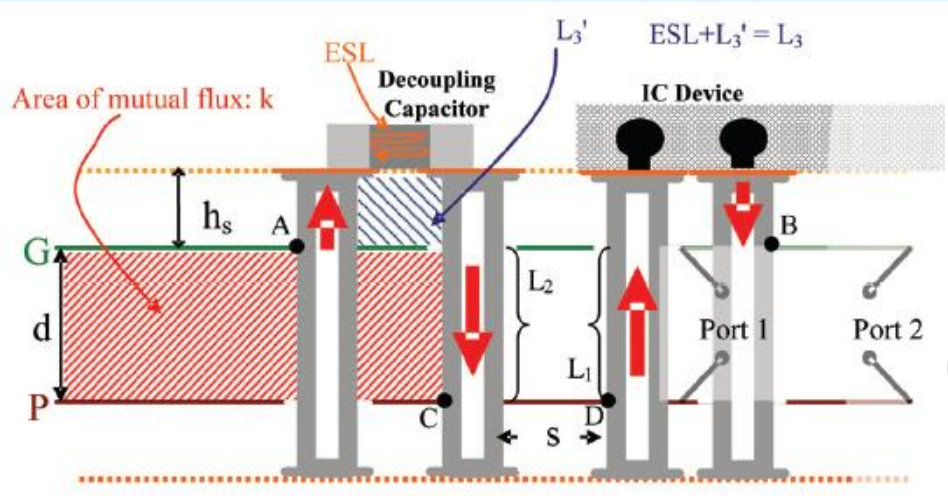
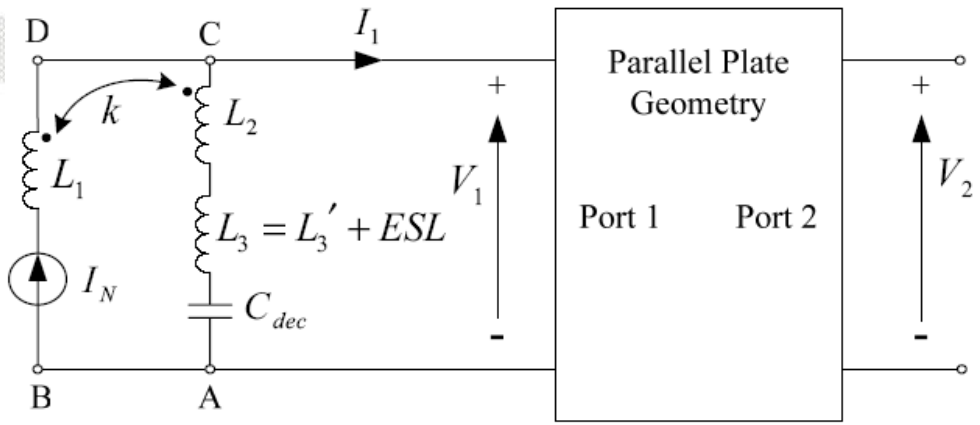


Figure 1: The inductance in the current path between IC and decoupling capacitor includes inductance elements above and below the planes, as shown by the regions of magnetic flux enclosed by the current path.

寄生電感對去耦合電容的影響

- 電容越靠近IC，由於互感L_{12}越小，所以總迴路電感越小，C效果越好
  - 並不是所有情況電容擺越近一定越好。當L_{below}不是主要電感成份時，電容擺近的改善就不大
  - $L_{below}=L_1+L_2-2*L_{12}$





多層板IC旁的電源去耦合電容

- 多層板時，如果(P,G)不是配置在中間層位置，那去耦合電容擺放上層或下層就會大大影響電容的效果，因為擺錯層會導致L_{above}增加(因迴路面積增加)，此時L_{above}的影響會比L_{below}大

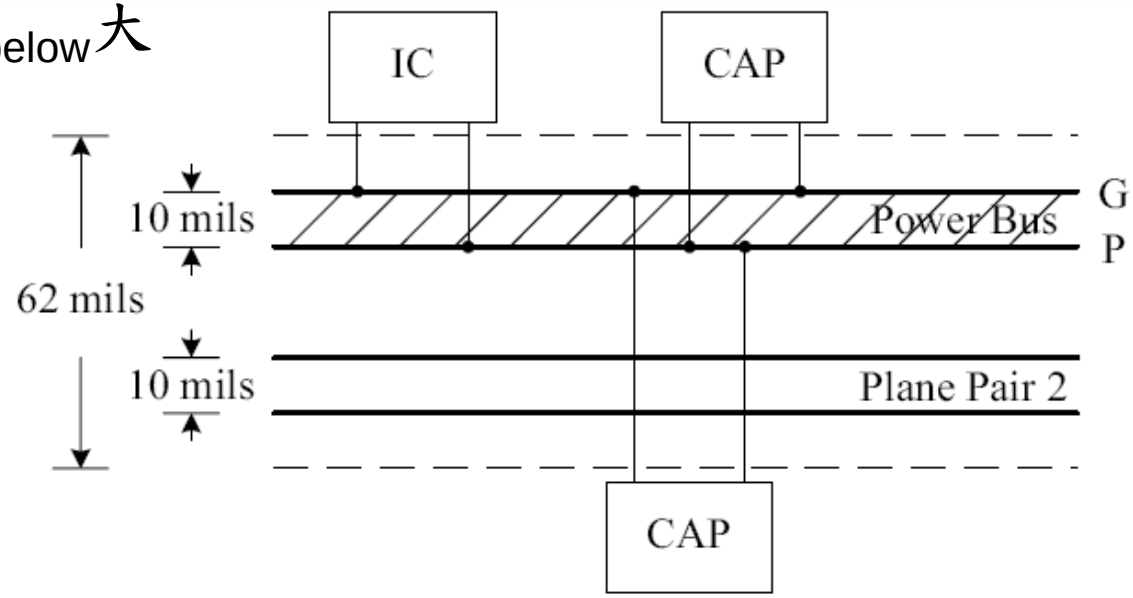
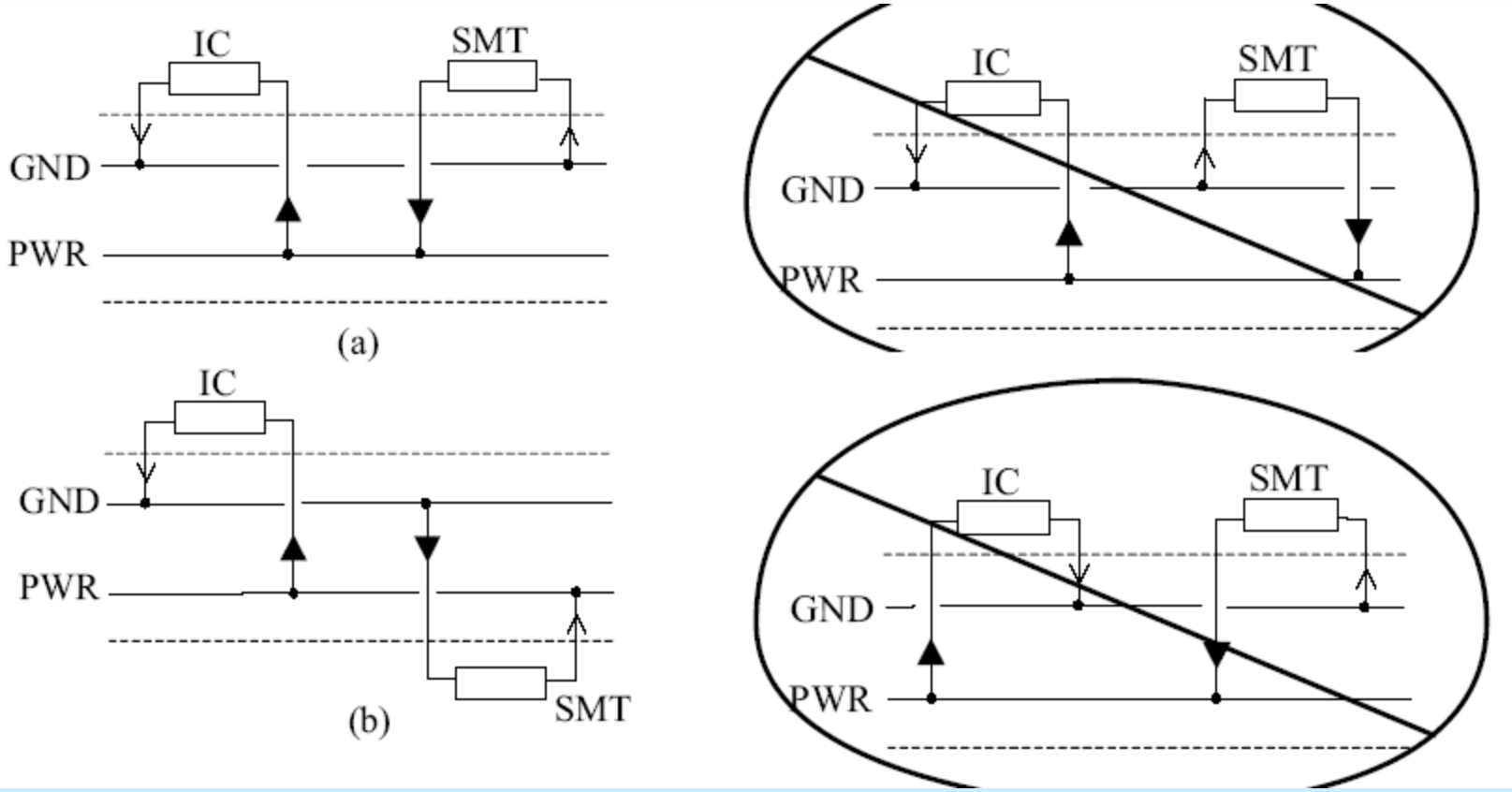


Figure 12: When power buses are moved away from the center of the stack-up, the L_3/L_2 inductance ratios are asymmetric and depend greatly on the surface on which the decoupling capacitor is placed.

降低電源去耦合電容的方法

- via間的互感增加(loop area小)，使L_{below}降低



降低電源去耦合電容的方法

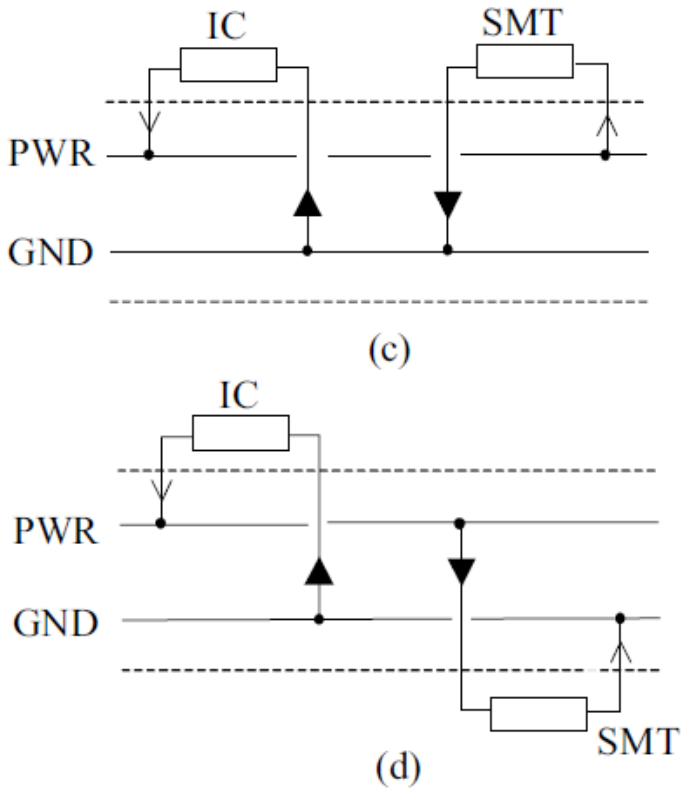


Figure 13: Examples of effective placement of SMT decoupling capacitors and proximate IC power/ground pins on a PCB power bus. The close proximity of the longer via lengths increases the mutual coupling between the vias and enhances local decoupling behavior.

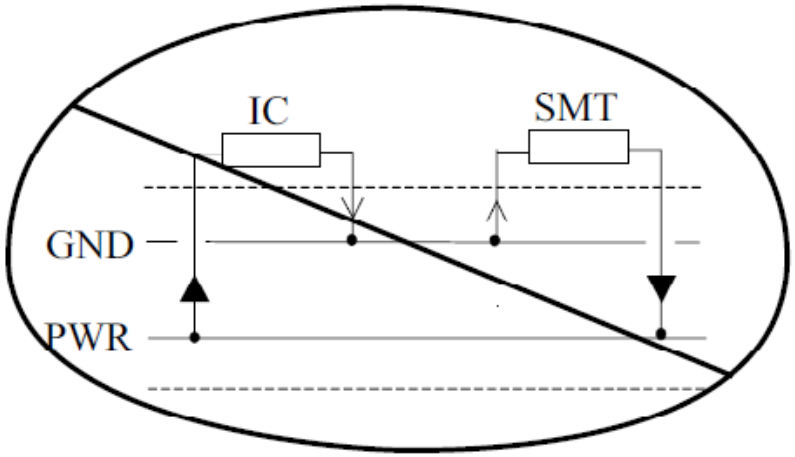
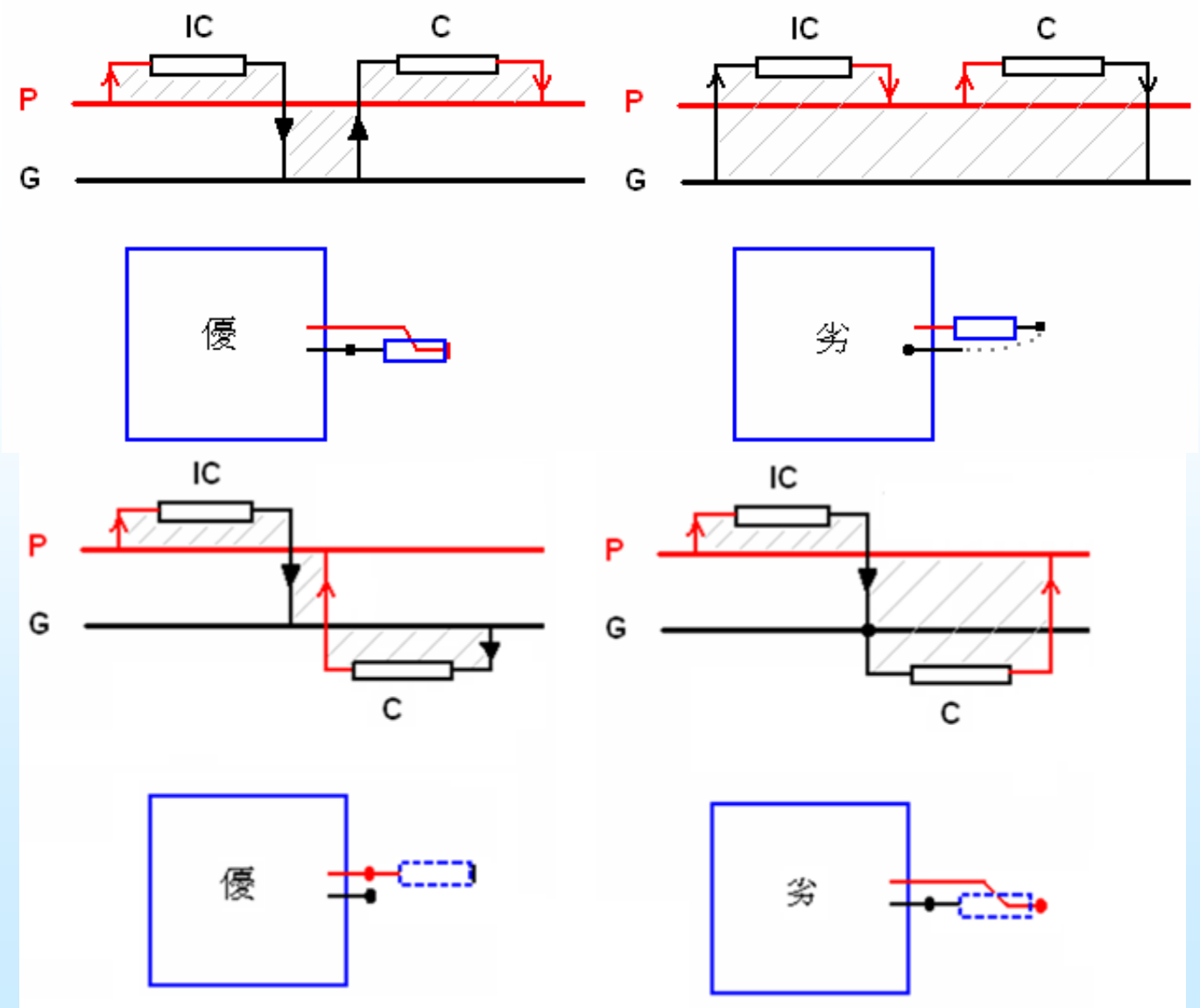


Figure 14: Examples of the three incorrect combinations of placement of IC and capacitor, corresponding to Figure 13(a). Each of the remaining three "right" configurations in Figure 13 have three "wrong" configurations that can be deduced from this figure.

兩層板電源去耦合電容最佳擺法



總結

- 寄生電感影響電源去耦合電容的效果
- 把去耦合電容靠近IC以降低L_{below}
- 多層板時，器件盡量連接到最近的(P,G)，以使去耦合電容能得到最小的L_{above}
- 高頻電路用的電源，特別需要注意