Electromagnetic Compatibility (*EMC*)

ESD Strategies in IC and System Design

Agenda

- *ESD Design in IC Level (摘錄自柯明道教授的網頁)*
  - Design Guide Lines
  - CMOS Design
    - Process Level Method
    - Circuit Level Method
  - Whole Chip Design
    - Internal Damage
    - Vdd-Vss Protection
    - Mix-Mode IC
- ESD Design in System Level
  - Equipment Design
  - Software Design

Design Guide Lines

Design Considerations on ESD Protection Circuits

- *Provide the IC with efficient discharging paths to bypass any ESD stress while the IC is in the ESD-stress conditions.*
- *Pass the normal I/O signals and keep inactive while the IC is in normal operating conditions.*
- Low input capacitance and resistance to meet acceptable I/O signal delay. (as small as possible)
- Have a high ESD robustness within a reasonable layout area. (as small as possible)
- Maintain a high latch-up immunity in the CMOS IC (all the I/O devices and ESD protection devices must be surrounded by guard rings).
- Fabrication of such ESD protection devices can be compatible to the process technology (without increasing additional mask layers or modifying the process steps as possible)
- High-voltage-tolerance I/O applications. The snapback holding voltage of the ESD clamp devices should be greater than the maximum voltage level of the input signals.

Design Guide Lines

VDD

Internal Circuits

PMOS

NMOS

Input PAD

ESD Protection Circuit

ESD Protection Circuit

ESD Protection Circuit

ESD Protection Circuit

Output PAD

ESD Protection Circuit

VSS

Inupt Protection

Input Buffer

Output Buffer

Outupt Protection

VDD-to-VSS Protection

- ESD protection circuit can not work in normal mode.

Design Guide Lines

Unexpected Discharging Path
ESD Current Discharging Path
VDD PAD
Rdd
PMOS
Input PAD
ESD Protection Circuit
C (VDD-to-VSS)
ESD Protection Circuit
NMOS
0V
-Vp
VSS PAD
Rss
ND-mode ESD Voltage
Input Protection
Internal Circuits
Internal Circuits
VDD-to-VSS Protection

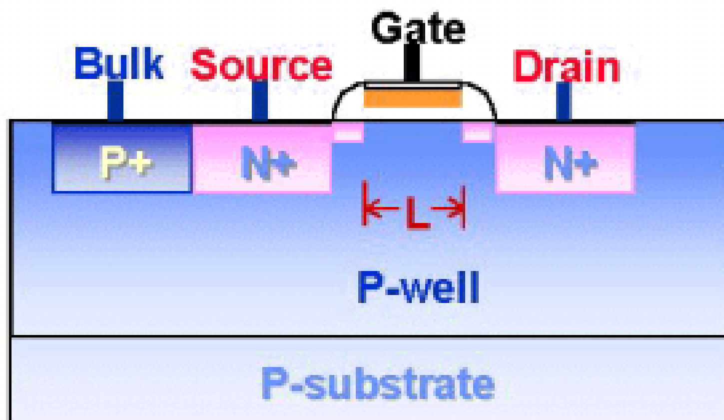
- Internal damage because of improper design.

CMOS Design

Process Level Method

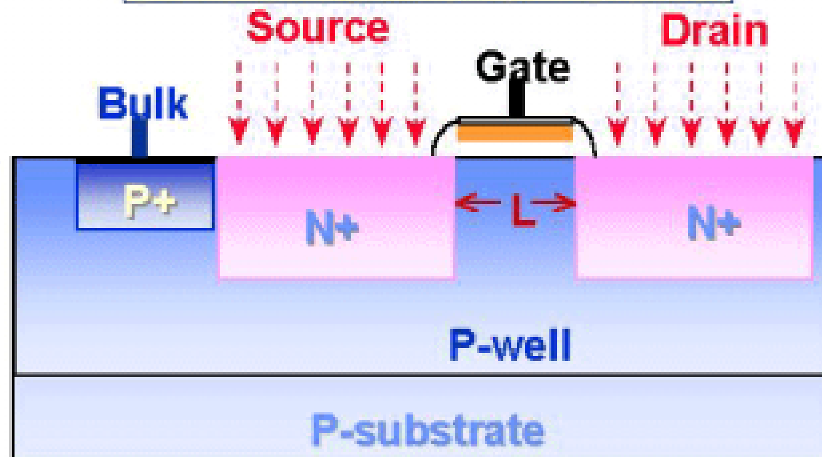
ESD Implant

LDD Structure



L = 1.0μm
Junction depth = 0.18μm
HBM ESD Robustness = 1KV

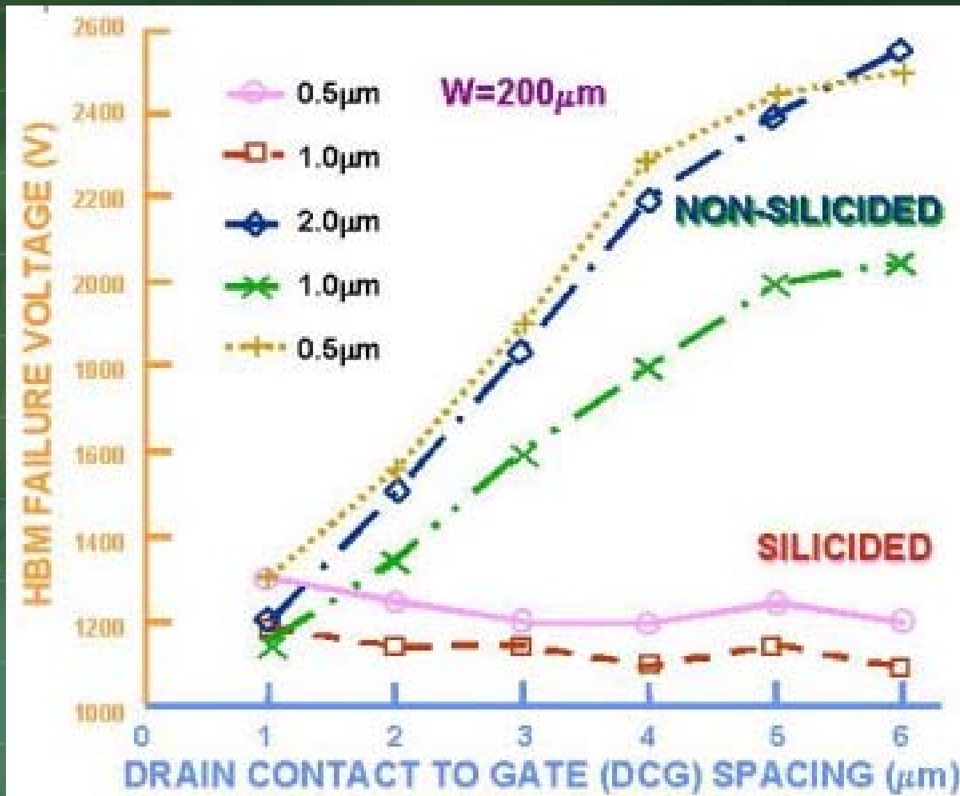
ESD-Implant Structure

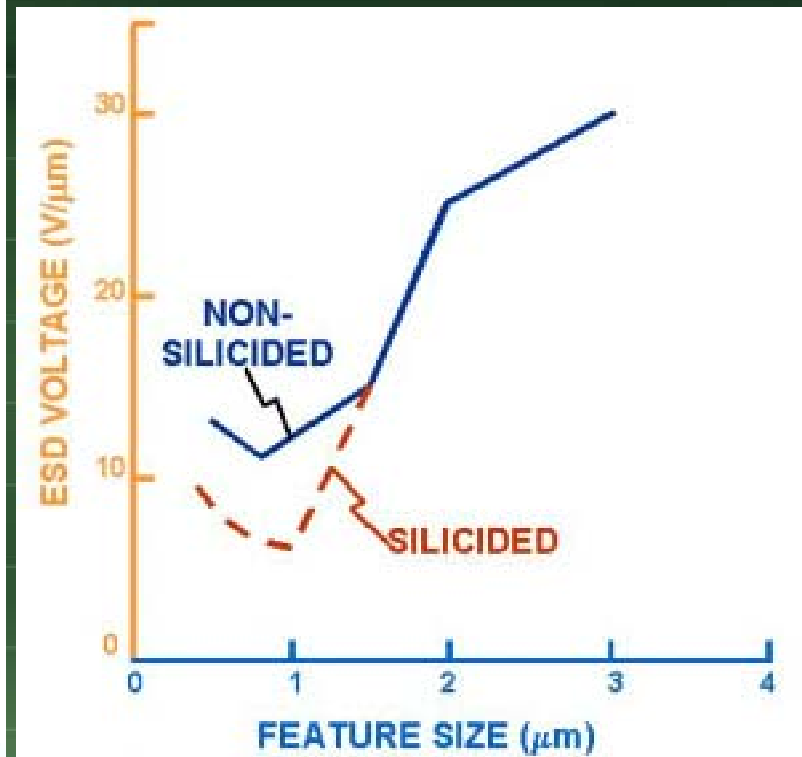


L → 1.4μm
Junction depth = 0.22 ~ 0.25μm
HBM ESD Robustness = 4KV
(0.6-μm CMOS Process)

CMOS Design

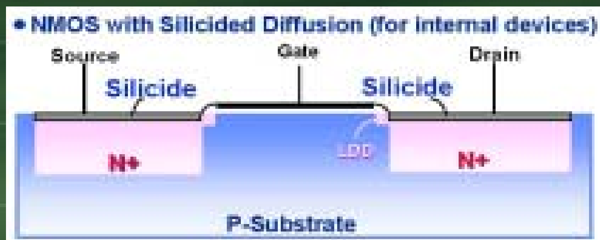
Process Level Method

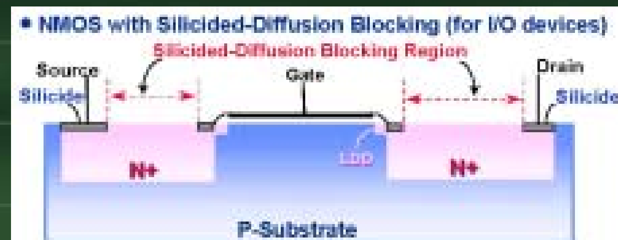


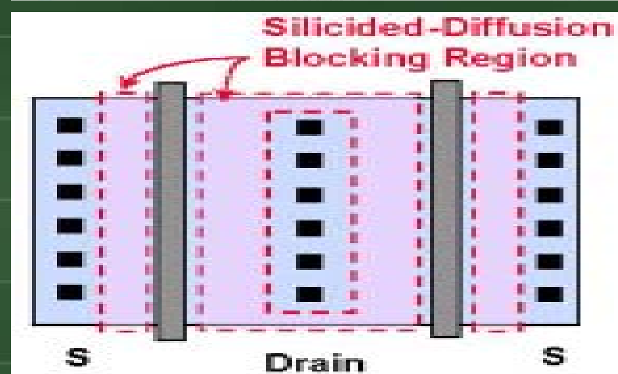


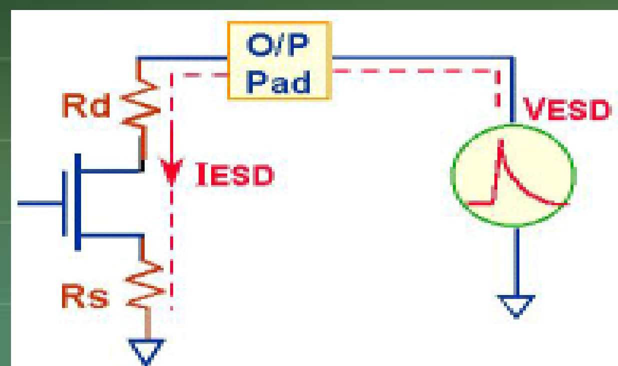
CMOS Design

Silicided-Diffusion Blocking

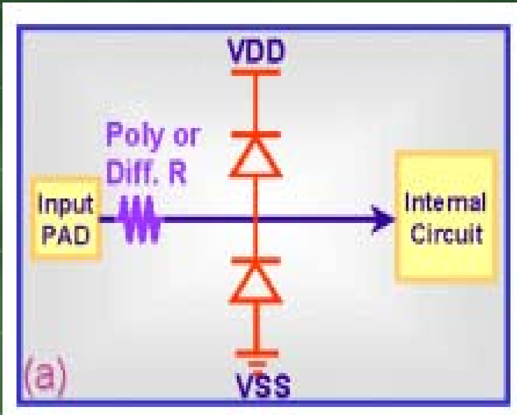


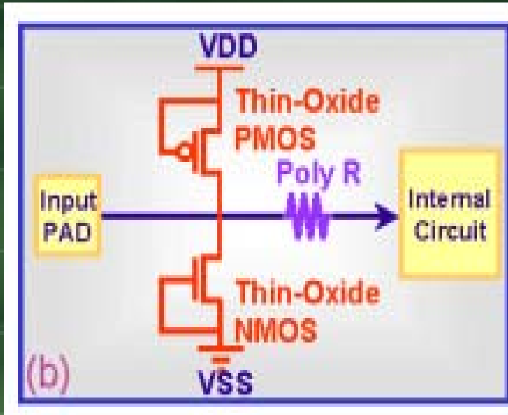


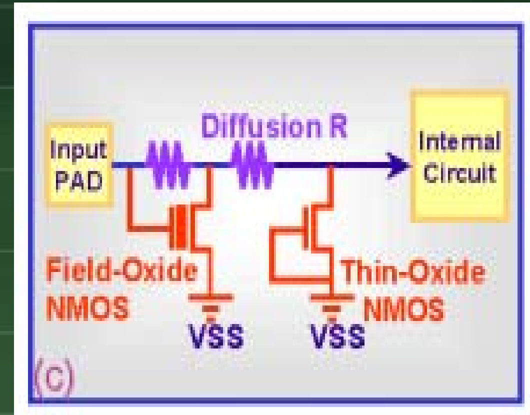


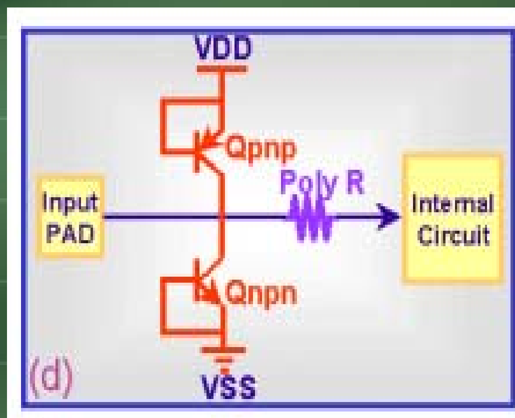


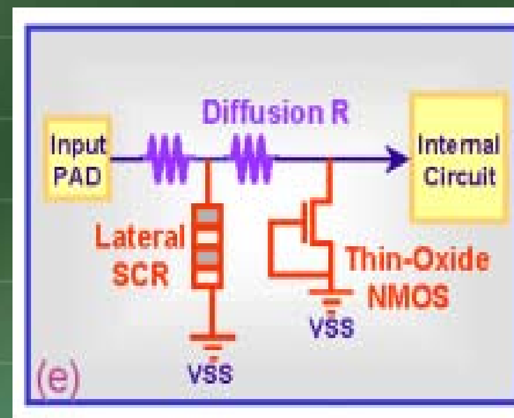
CMOS Design
Circuit Level Method





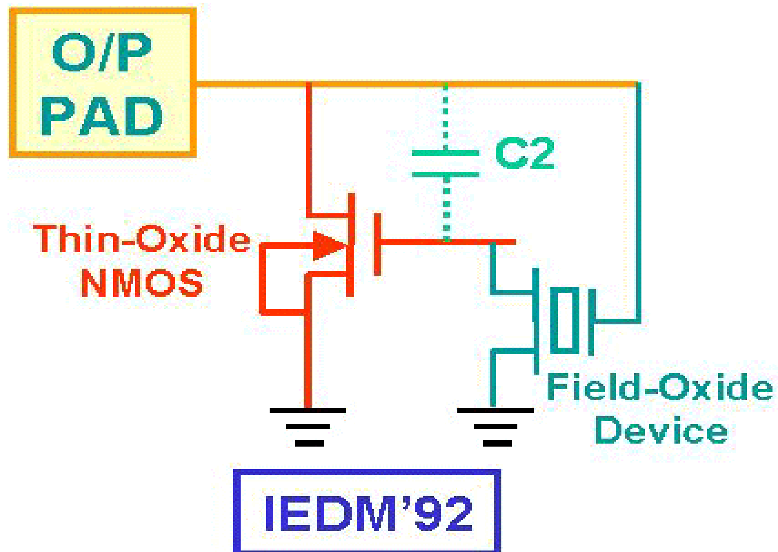


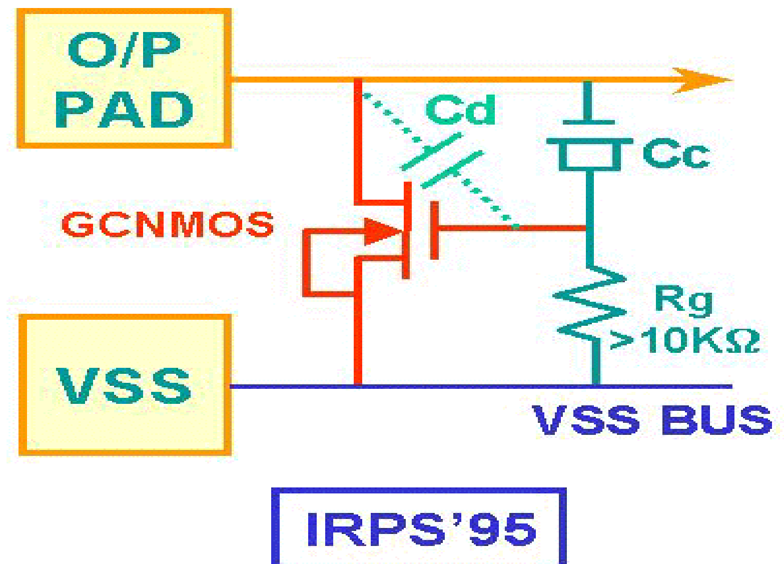




CMOS Design

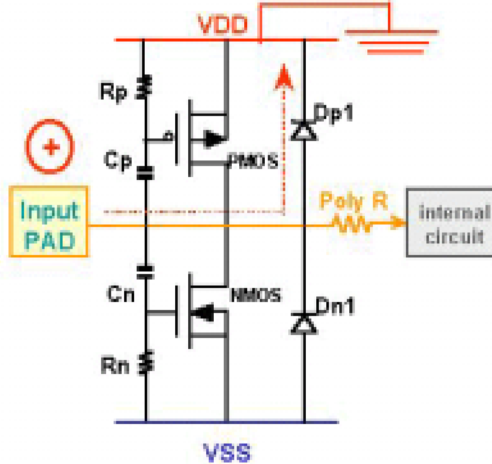
Circuit Level Method

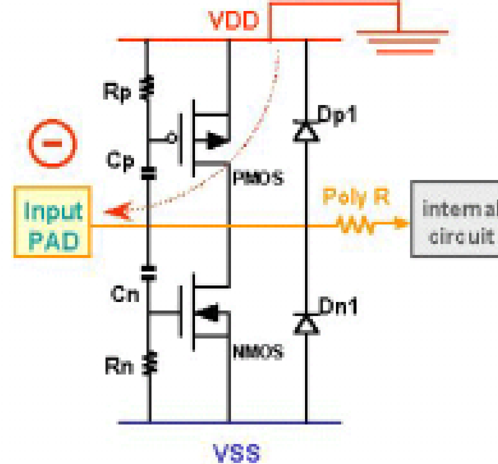


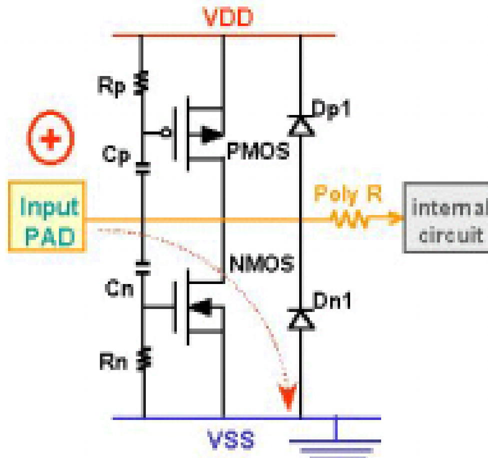


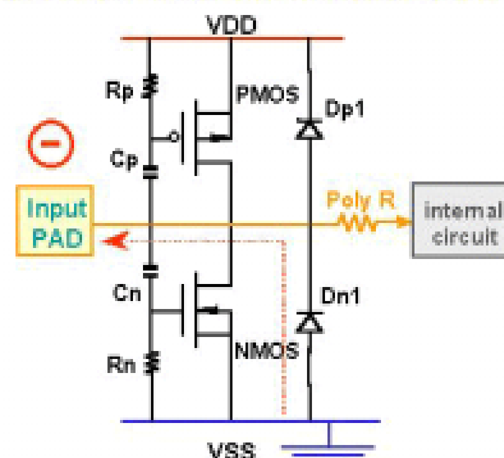
CMOS Design

Circuit Level Method









Whole Chip Design

Internal Damage

Internal ESD Damages under ND-mode ESD Stress on Output Pin

Unexpected Discharging Path

VDD PAD

R_{DD}

Input PAD

P
n
p
n

C
(VDD-to-VSS)

ESD Protection Circuit

ESD Protection Circuit

VSS PAD

0V
-V

ND-mode ESD Voltage

Input ESD Protection

Internal Circuits

Parasitic Field-Oxide Device

VDD-to-VSS Latchup Path

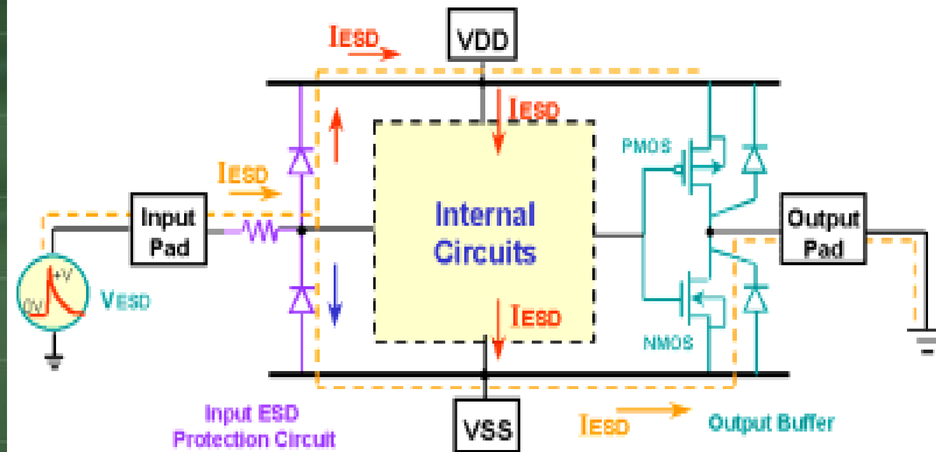
Internal Circuits

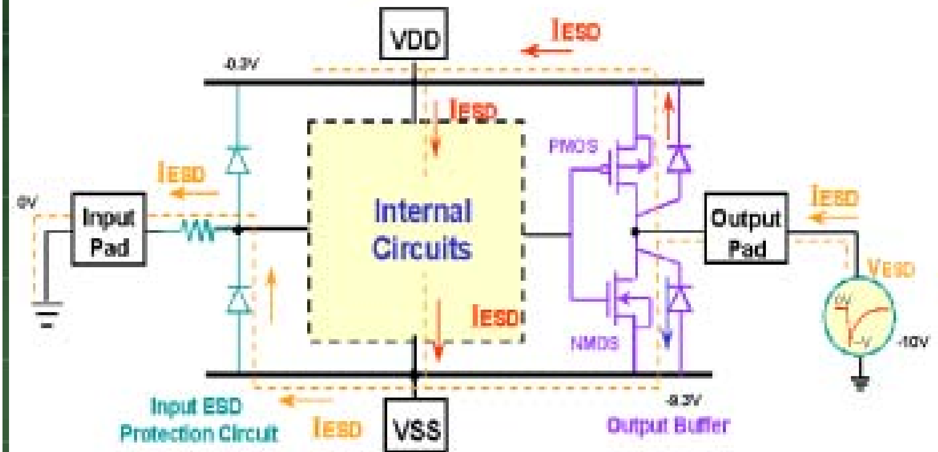
R_{SS}

VDD-to-VSS Protection

Whole Chip Design

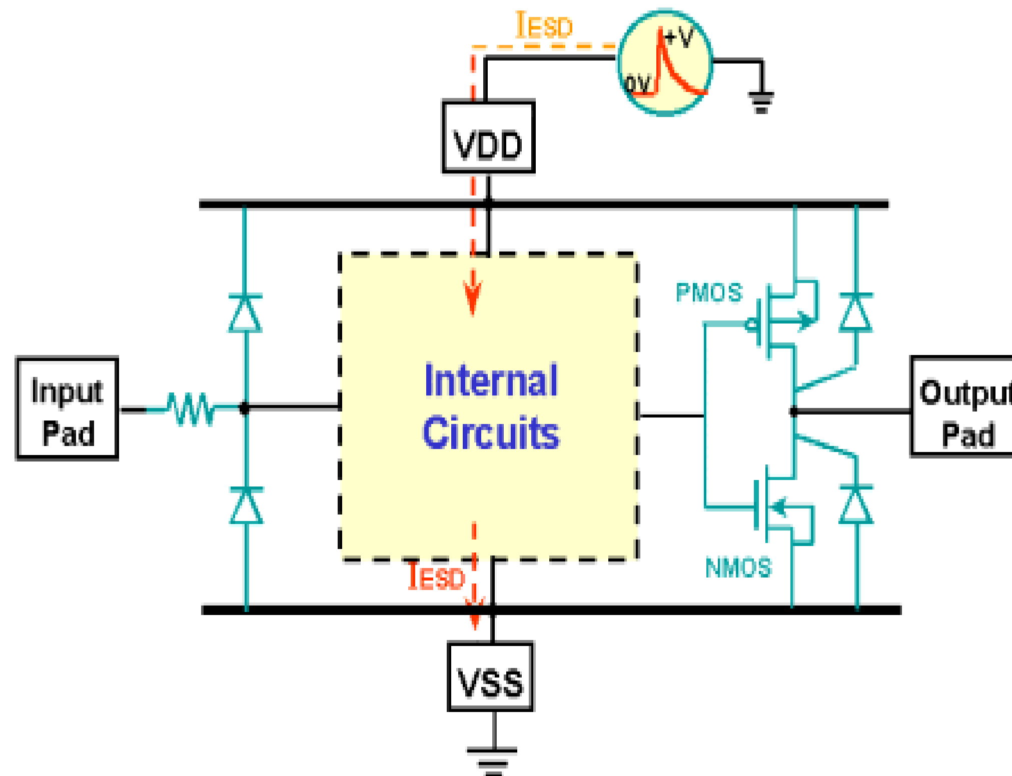
Internal Damage due to Pin-to-Pin ESD





Whole Chip Design

Internal Damage due to V_{DD}-Vss ESD

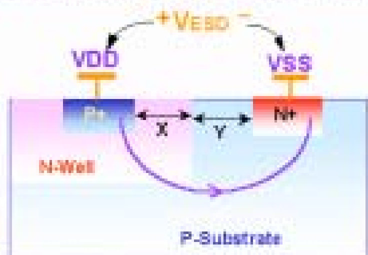


Whole Chip Design

VDD-Vss Protection – Parasitic SCR and BJT

Layout Spacings in the Scaled-Down CMOS Process

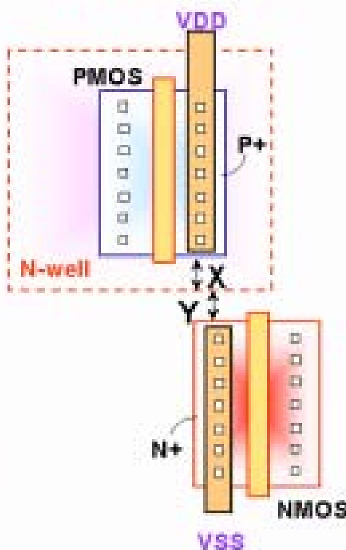
- Cross-Sectional View of the Latchup Path



- Minimum Spacings in the Design Rules

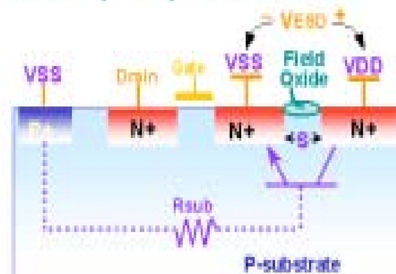
TSMC Process	X (µm)	Y (µm)	X+Y (µm)
0.8-µm	2.4	2.4	4.8
0.6-µm	1.8	1.8	3.6
0.5-µm	1.5	1.5	3.0
0.35-µm	1.2	1.2	2.4
0.25-µm	0.6	0.6	1.2

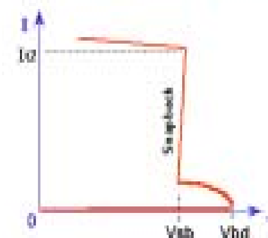
- Layout Example



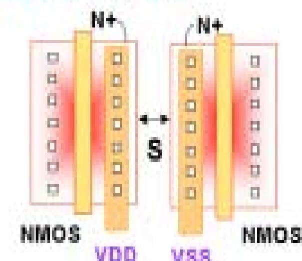
Lateral n-p-n BJT in the Scaled-Down CMOS Process

- Cross-Sectional View of the parasitic lateral n-p-n bipolar transistor





- Layout Example



- Specified minimum spacing

TSMC Process	S (µm)
0.8-µm	1.6
0.6-µm	1.2
0.5-µm	0.9
0.35-µm	0.6
0.25-µm	0.4

- Parasitic SCR and BJT in CMOS are easy to be damaged while ESD current appears.

Whole Chip Design

VDD-Vss Protection

Prior Art of VDD-to-VSS ESD Protection

- A gate-grounded NMOS is used as the ESD clamp device between the VDD and VSS Power lines

Whole Chip Design

VDD-Vss Protection

Effective VDD-to-VSS ESD Protection Design

- Under the ESD-stress condition, the NMOS provides a short-circuit path between the VDD and VSS power lines.

Whole Chip Design

Issue of Parasitic Resistance and Capacitance along the VDD/VSS Power Lines

Spacing ?

Spacing ?

VDD

Rdd

Dp1

PMOS

Dp2

R

Input Pad

Internal Circuits

Output Pad

Cds

C

Dn1

NMOS

Dn2

VSS

Rss

VDD-to-VSS ESD Protection Circuit

➡ The width of VDD/VSS Power lines is an important design parameter.

Whole Chip Design

Test Chip to Verify Spacing Effect on ESD Protection

Output Pad

Input Pad

Spacing

Spacing

30μm

Output Pad

Output Pad

......

Output Pad

Output Pad

VSS

VDD

ESD Clamp

Input Pad

Input Pad

Input Pad

......

Input Pad

Input Pad

30μm

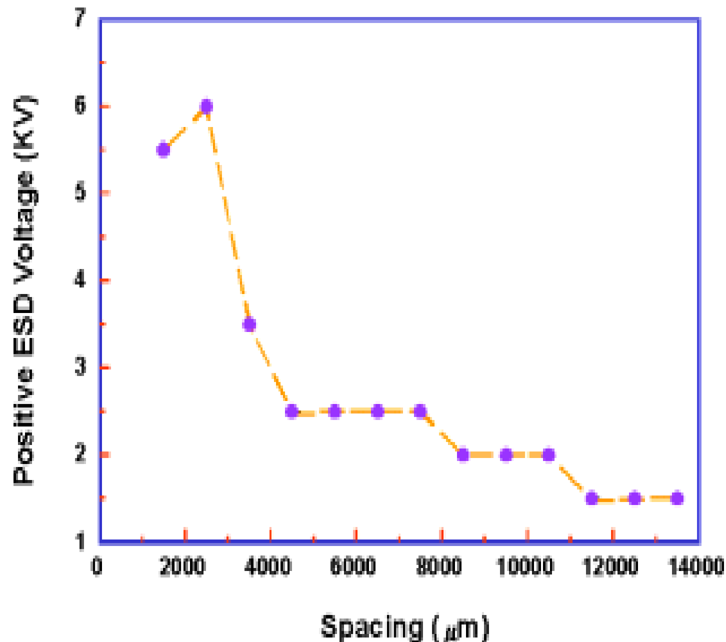
Output Buffer
PMOS=150/1.2
NMOS=150/1.2

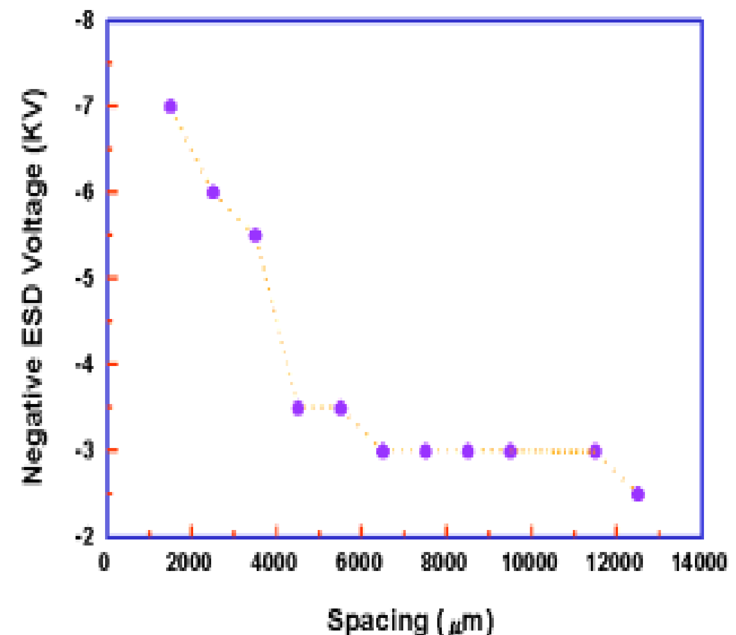
W/L=250/1.4
R=100KΩ
C=2pF

Input ESD
Dp=120/2.4
Dn=120/2.4

- Fabricated in a 0.8-μm CMOS process.

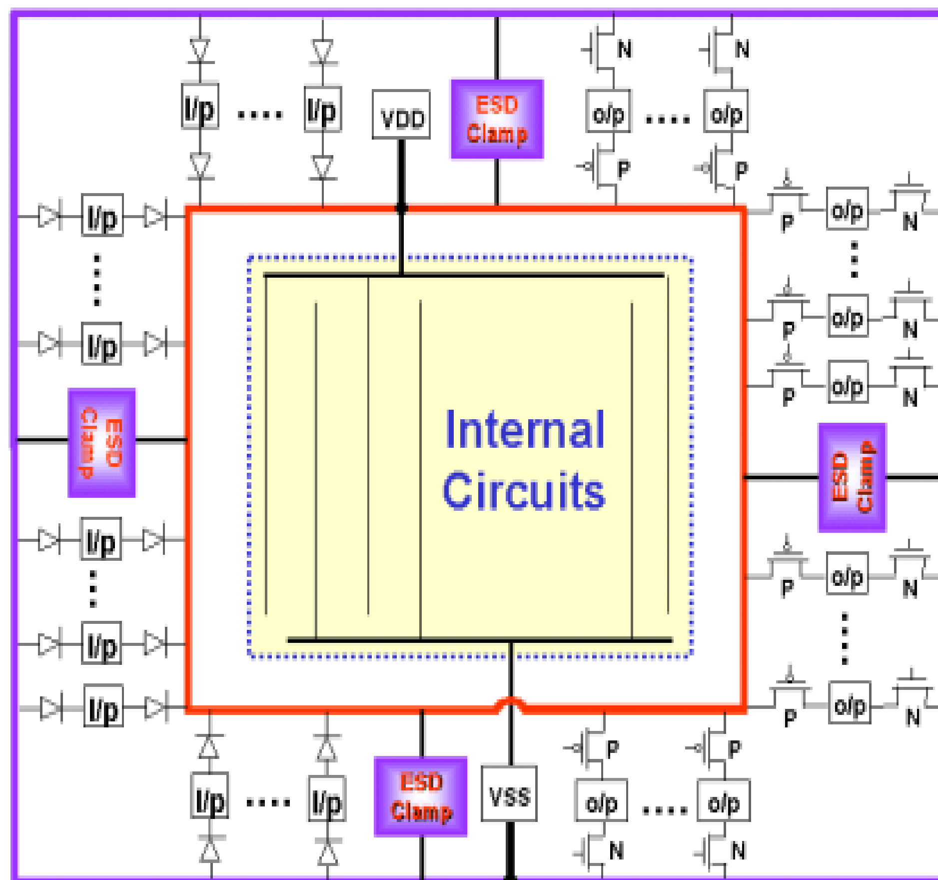
Whole Chip Design





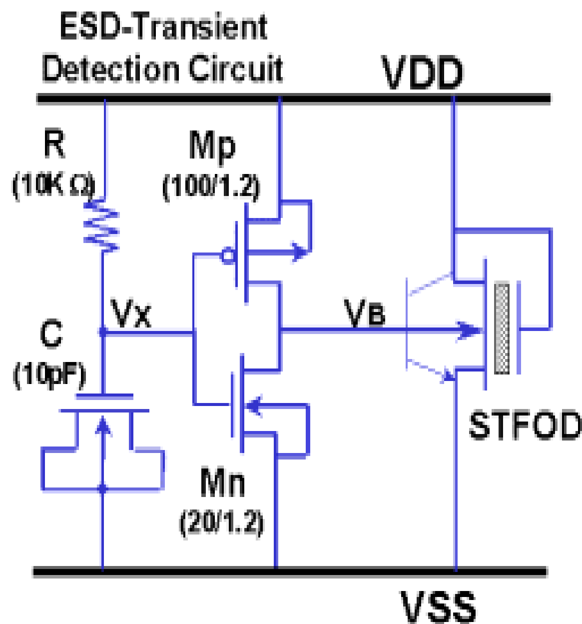
- It is better to keep the length of power lines between I/O cell to VDD-Vss ESD clamp less than 2000μm with 30μm width.

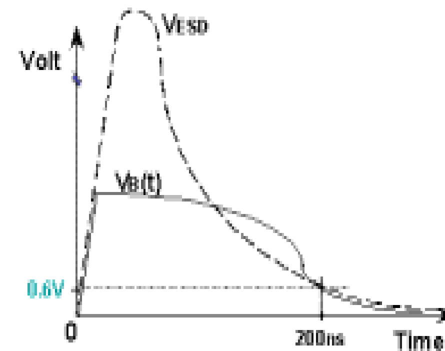
Whole Chip Design

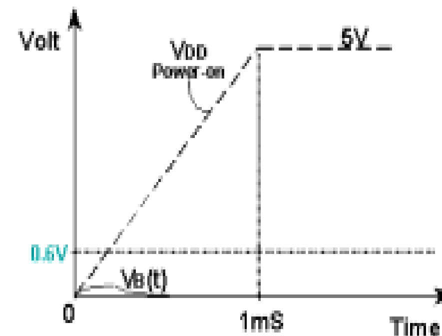


Whole Chip Design

Area-Efficient VDD-to-VSS ESD Clamp Circuit by Using the Substrate-Triggering Field-Oxide Device (STFOD)

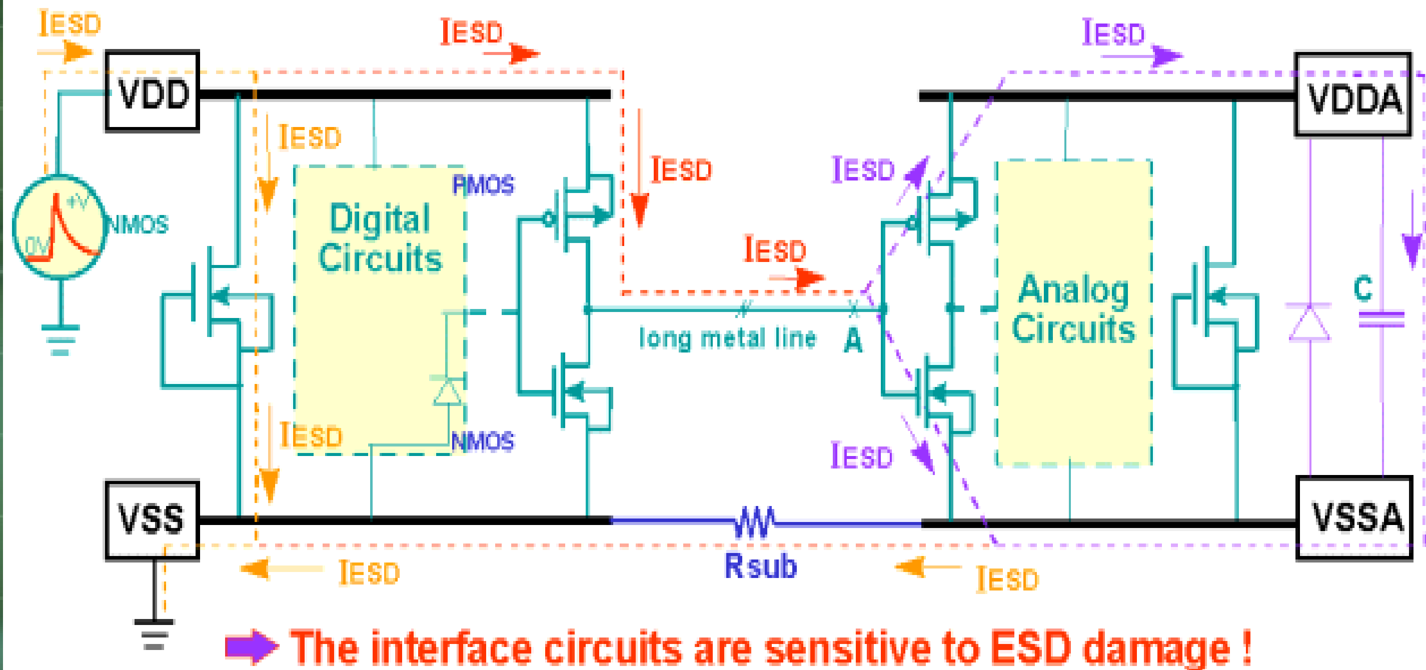






- The STFOD device provides a short-circuit path between the VDD and VSS power lines, when the ESD voltage is across between VDD and VSS.

Mix-Mode IC



Mix-Mode IC

ESD Current Discharging Paths during the Pin-to-Pin ESD Stress in a Mixed-Mode IC with ESD-Connection Diodes

- An ESD voltage occurs on a digital input pin with an analog output pin grounded, but all the digital and analog power pins are floating.

Agenda

- ESD Design in IC Level
  - Design Guide Lines
  - CMOS Design
    - Process Level Method
    - Circuit Level Method
  - Whole Chip Design
    - Internal damage
    - Vdd-Vss Protection
    - Mix-Mode IC
- *ESD Design in System Level*
  - Equipment Design
  - Software Design

ESD Design in System Level

- Energy from ESD can be coupled to an electric circuit in two ways
  - By direct conduction
    - This often results in damage to the circuit
  - By capacitive or inductive coupling
    - They occur when there is a discharge to a nearby metal object or cable, and the resulting fields are coupled to the susceptible circuit.

ESD Design in System Level

- I/O cable treatment
  - Use of cable shielding
  - Common-mode chokes
  - Over-voltage clamping devices
  - Cable with bypass filters
- Taking care of ESD noise invaded
  - Recheck critical inputs (several ms apart)
  - Use less sensitive and slow (narrow bandwidth) devices
    - Use differential I/O schemes
    - Do not use edge-triggered or wide bandwidth logic

Equipment Design

Manufacturing and Installation Guidelines

- Eliminating the static buildup on the source.
  - Using the poor charge generators (dielectric materials) as an enclosure
- Protecting a sensitive circuit from ESD
  - Insulating the product to prevent a discharge.
  - Providing an alternative path for the discharge current to bypass the circuit.
- Shielding the circuit against the electric fields produced by the discharge.
- Protecting the circuit against the magnetic fields produced by the discharge.

Equipment Design

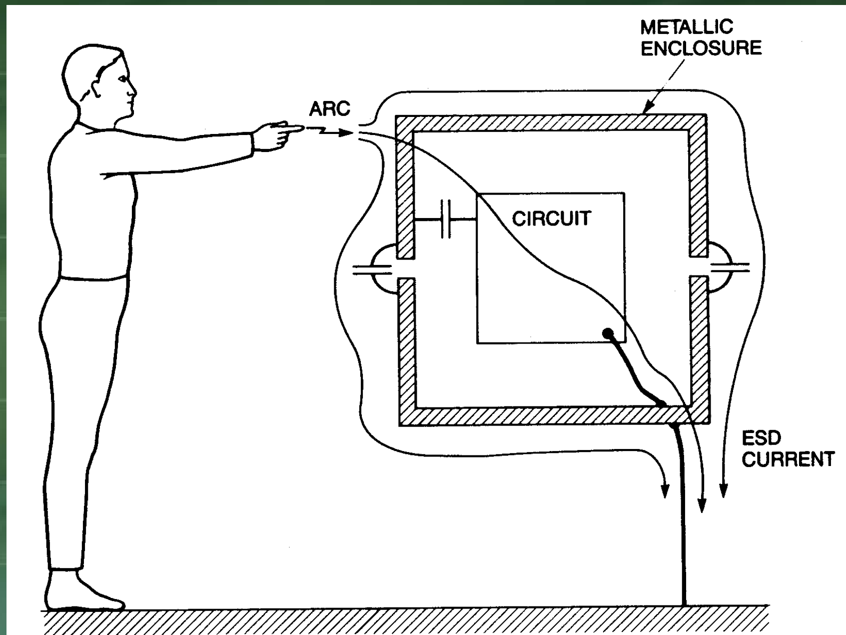


Figure 12-7. *Electrostatic discharge to a metallic enclosure that does not have electrical contact across the seams.*

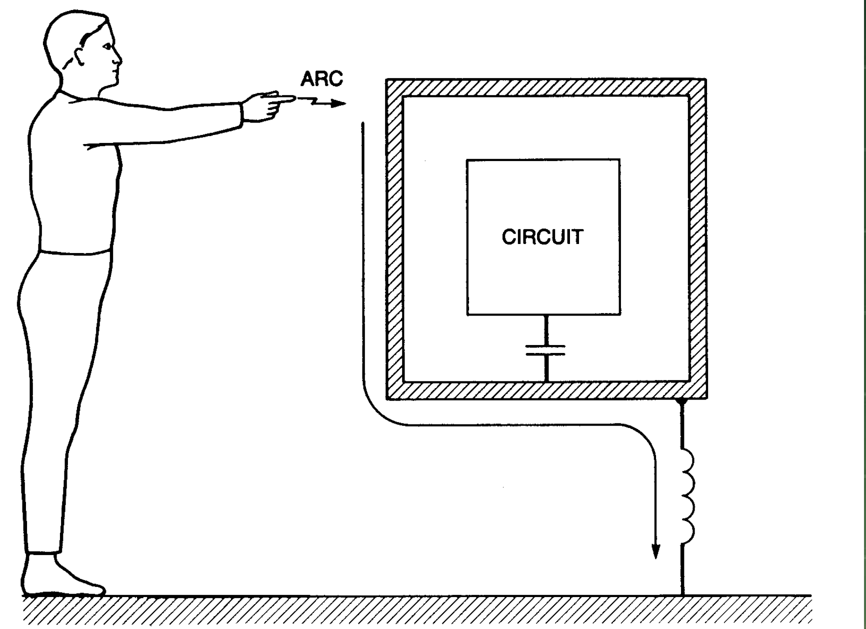


Figure 12-8. *Electrostatic discharge to a metallic enclosure that completely encloses a circuit. The circuit has no external connections.*

Equipment Design

SECONDARY SHIELD
CONNECT TO CKT. COMMON

PWB

PWB

(A)

(B)

Figure 12-9. *Capacitive coupling between a metallic enclosure and a circuit (A). A secondary shield (B) can be used to block the capacitive coupling between a circuit and a metallic enclosure.*

Equipment Design

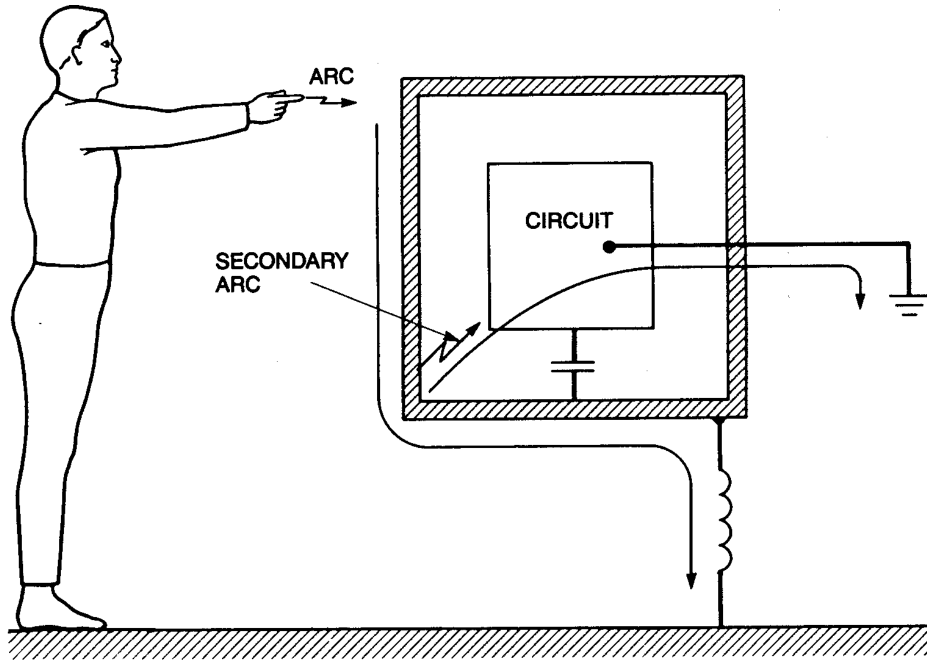


Figure 12-10. *Electrostatic discharge to a metallic enclosure containing a circuit with an external ground connection.*

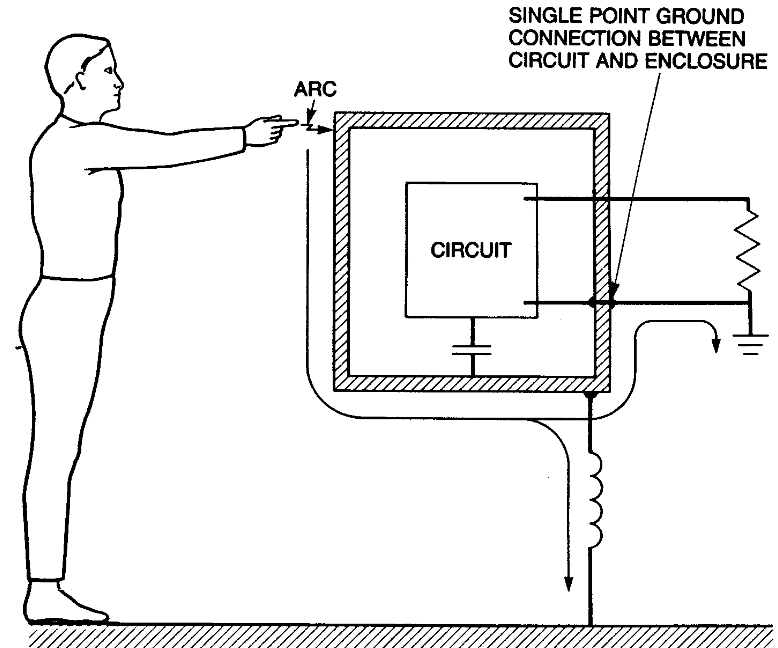


Figure 12-11. *Electrostatic discharge to a metallic enclosure containing a circuit with a single-point connection between the enclosure and the circuit.*

Equipment Design

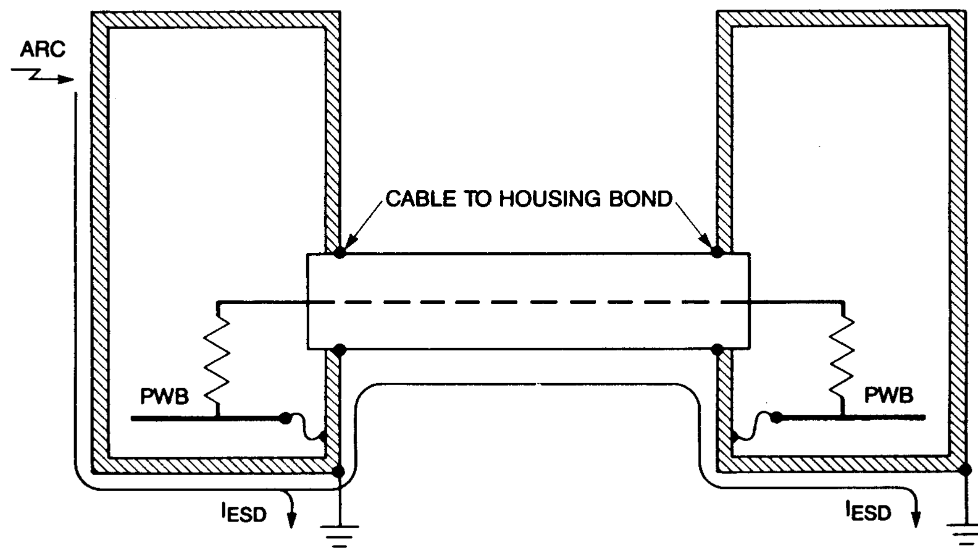


Figure 12-12. *Two enclosures connected with a shielded cable, in an attempt to turn the two into one continuous enclosure.*

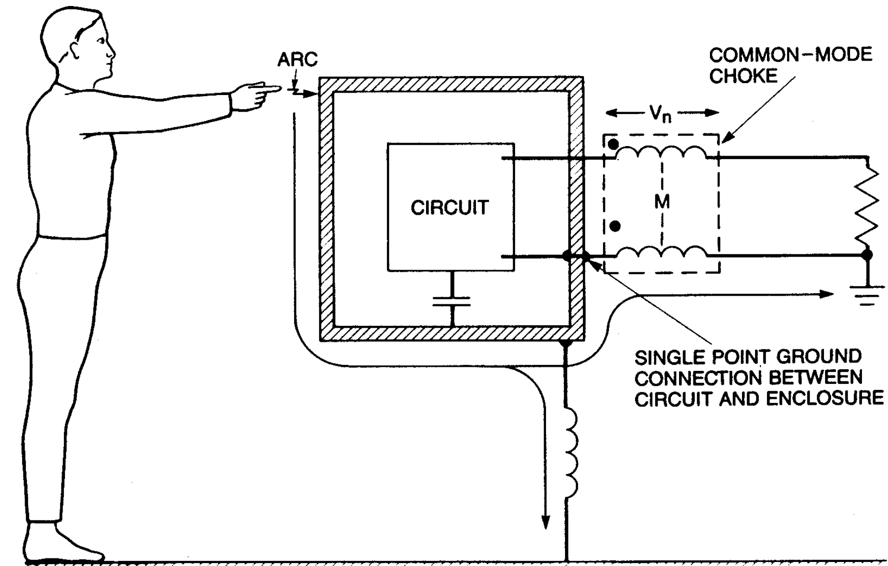


Figure 12-13. *A common-mode choke can be used on the interface cable to drop the ESD-induced noise voltage (V_N).*

Equipment Design

INPUT CABLE

INPUT CABLE

PWB

PWB

ESD CURRENT FROM CABLE

(A)

(B)

Figure 12-14. *Improper connection between PWB and chassis (A) forces ESD currents on cables to flow through the PWB. Proper connection (B) diverts ESD current from PWB.*

Equipment Design

INPUT CABLE

PWB

ESD CURRENT

INPUT CABLE

PWB

ESD CURRENT

Equipment Design

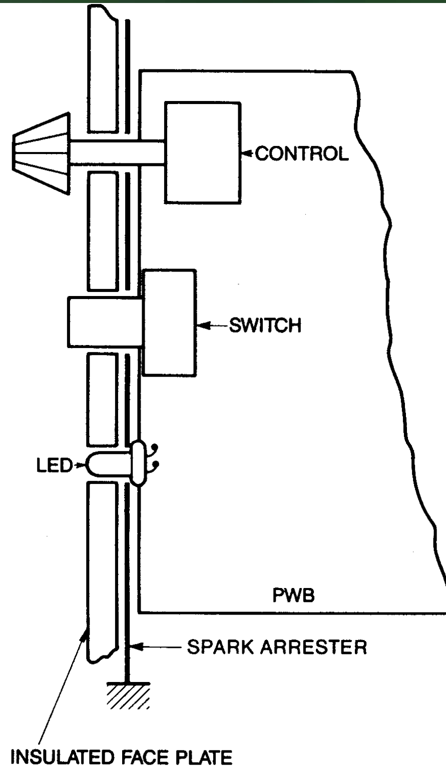
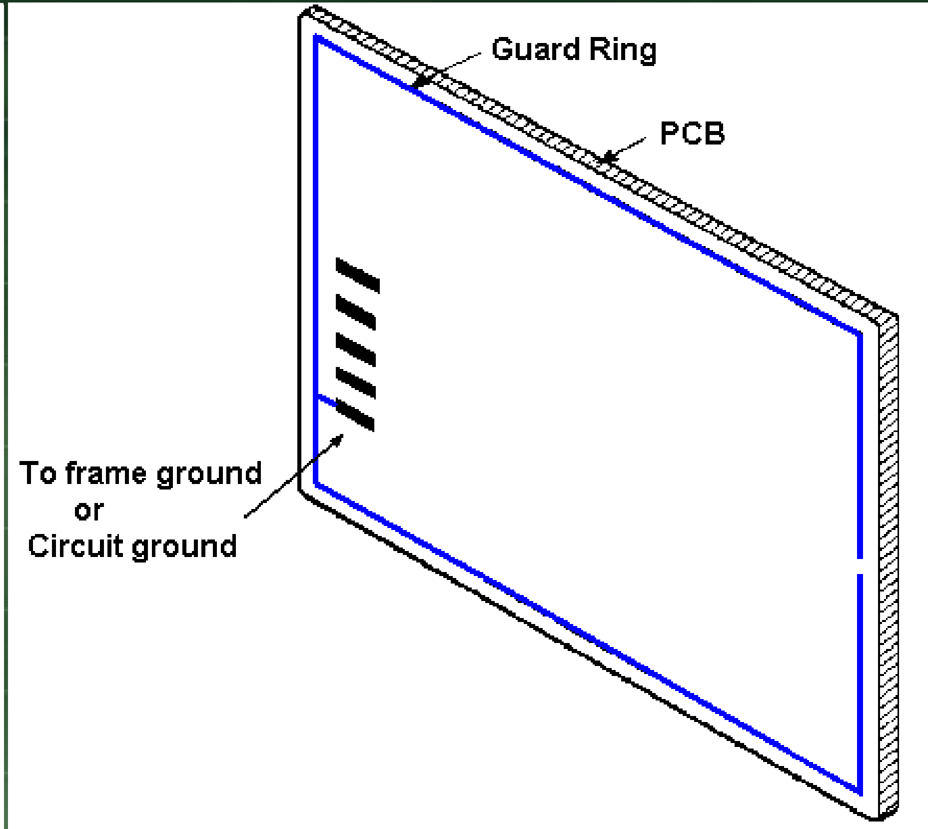
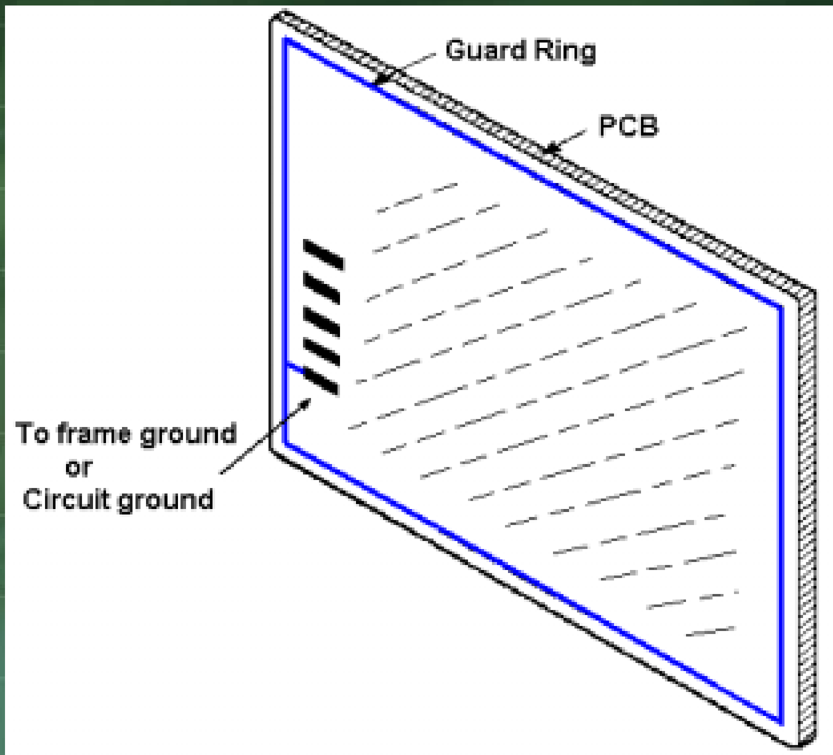


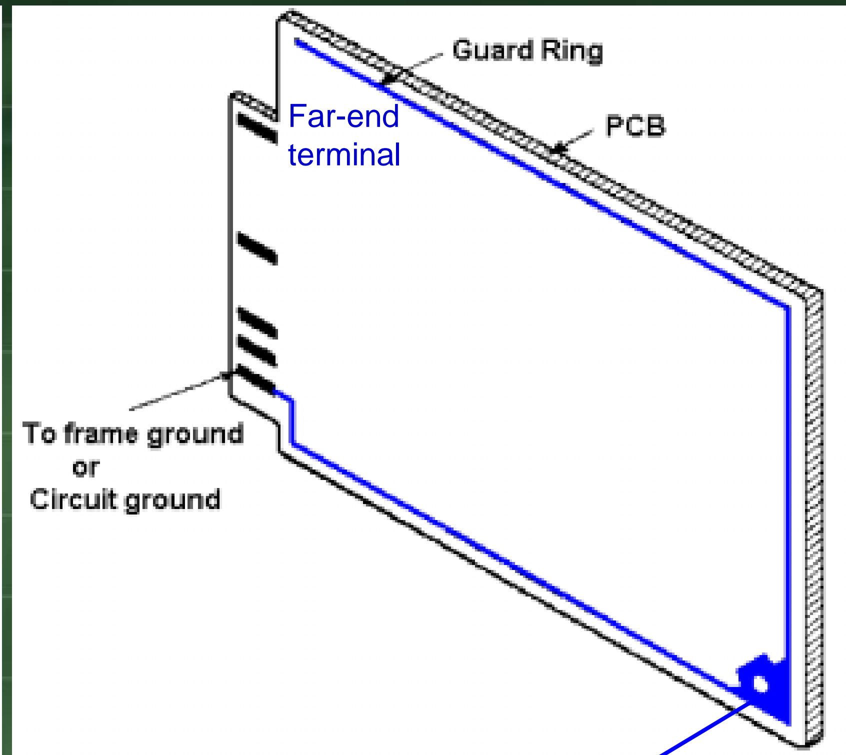
Figure 12-16. *Metallic spark arrestor placed behind an insulated face plate to divert the ESD current to ground.*



- *The guard ring must be naked and wide enough,* and it may be connected to circuit on board *or not.*

Equipment Design





- *The loop area formed by guard trace will be able to induce radiated interference. That is, it will be worse for RS test.*
- *Without case connecting point, the far-end terminal of the guard lead will have poor effect to drain ESD current.*

Equipment Design

Keyboard Example

- 使用防靜電袋(微導電性之靜電散逸材料)包裝成品，避免靜電累積
- 機構外部使用絕緣材料，防止靜電直接對內部電路放電破壞；機構內部則以導體所形成的guard wall或printed wires所形成的ground guard吸收殘餘的入侵靜電

Equipment Design

Keyboard Example

Cable

membrane

Keep a distance for ESD

VDD

GND

holes

PCB

screw

Seams on side

Software(Firmware) Design

- Detecting errors in program flow
  - Watch Dog Timer (WDT)
- Detecting errors in I/O
- Detecting errors in data memory
  - The values of SRAM in error or accessing faults to EPROM

Summary

- ESD hardening of a system involves the electric, mechanical, and software design of a system.
- All exposed metal must be grounded to chassis ground.
- Hardening a system against ESD will also make it immune to most other sources of radio-frequency interference.