Electromagnetic Compatibility (*EMC*)

Digital System and Circuit Design

Agenda

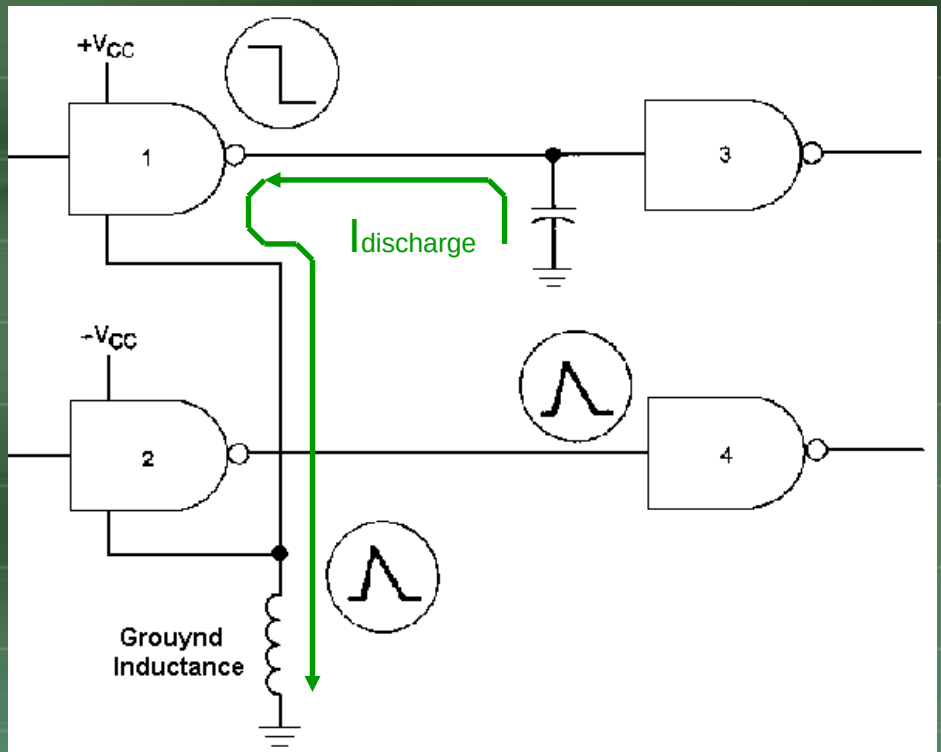
- *Digital Circuit Noise*
  - Frequency Domain
  - Ground Bus Noise
  - Power Bus Noise
  - Reflection Strategies
  - Crosstalk
  - PCB Technologies
- Digital Circuit Radiation
  - Differential-Mode Radiation
  - Controlling DM Radiation
  - Common-Mode Radiation
  - Controlling CM Radiation

Digital Circuit Noise

- A small integrated digital circuit, which draws only a few milliamperes, does not at first seem to be a serious source of noise. *However*, the high speed signals with the *inductance of leads*, make it a major source of noise.
- Digital-circuit designers think in terms of the time domain. Considering noise, however, it is better to think in terms of frequency domain.

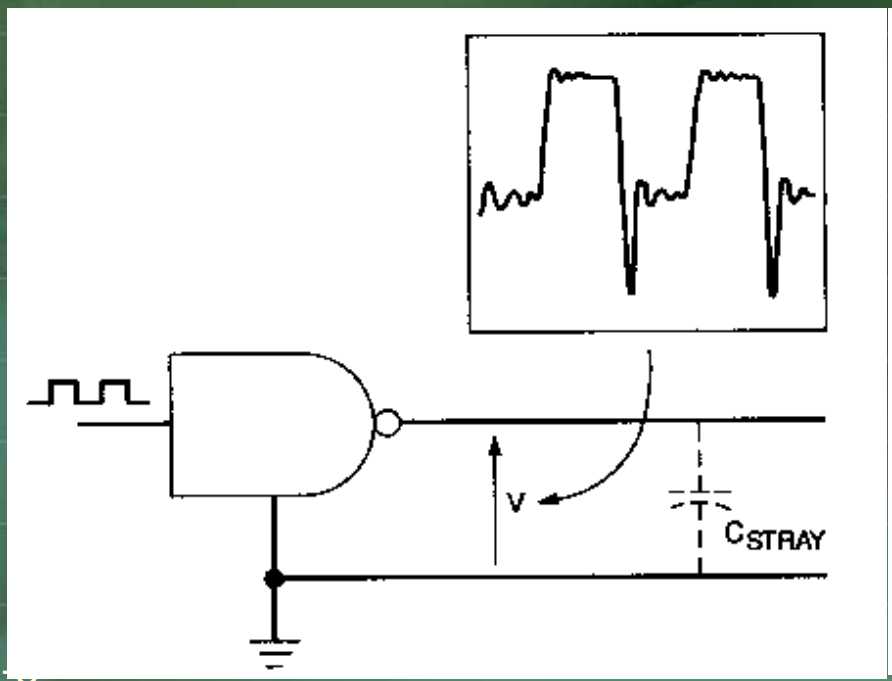
Digital Circuit Noise

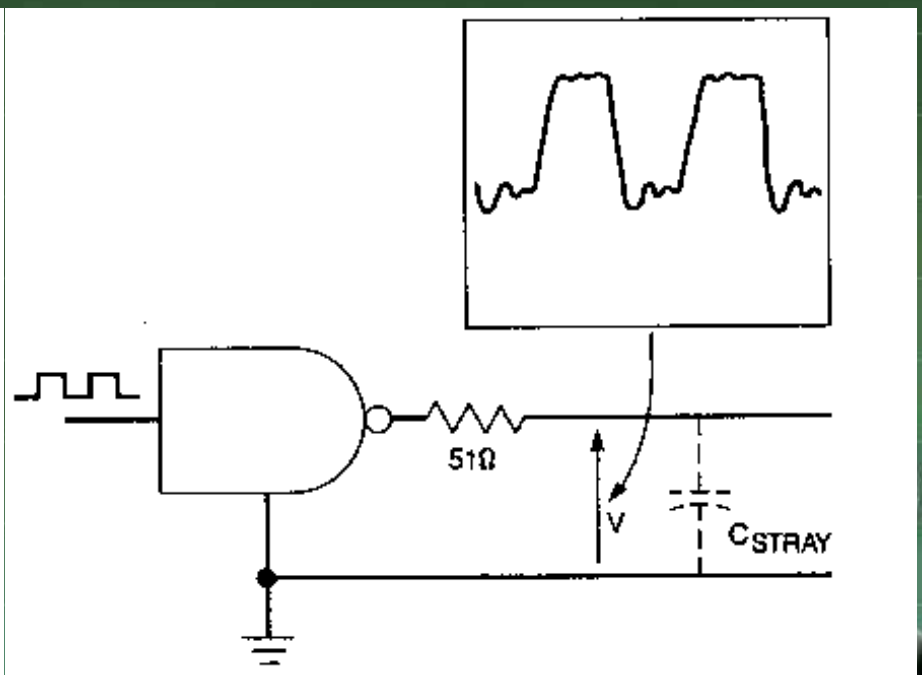
1. When gate 1 output transforms from high to low
2. C_{STRAY} is discharged
3. Therefore, a large transient current flows through the ground inductance to discharge C_{STRAY}.
4. Inducing noise on ground paths



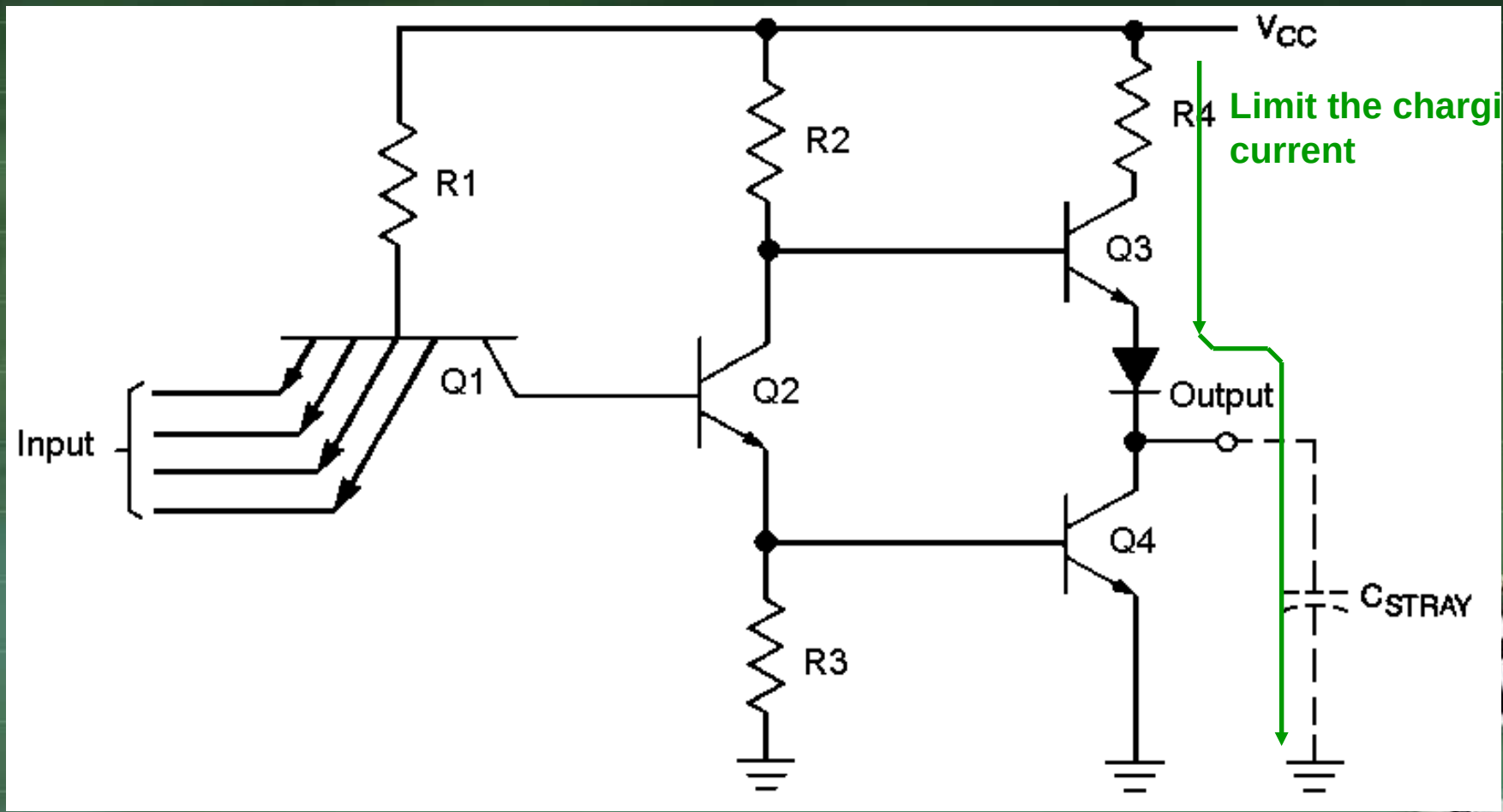
Digital Circuit Noise

- Adding damping with a resistor or a ferrite bead will decrease the ringing on gate 1 output.
  - Unwanted energy is dissipated as heat
- A back-biased diode also can clamp the negative voltage.
  - High current flows through the diode, which may cause additional noise problems





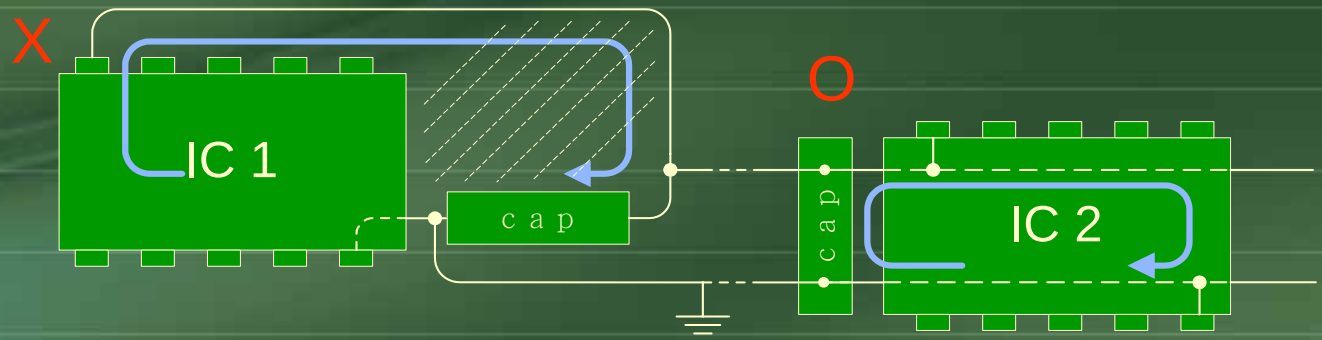
Digital Circuit Noise



Digital Circuit Noise

Design Strategies

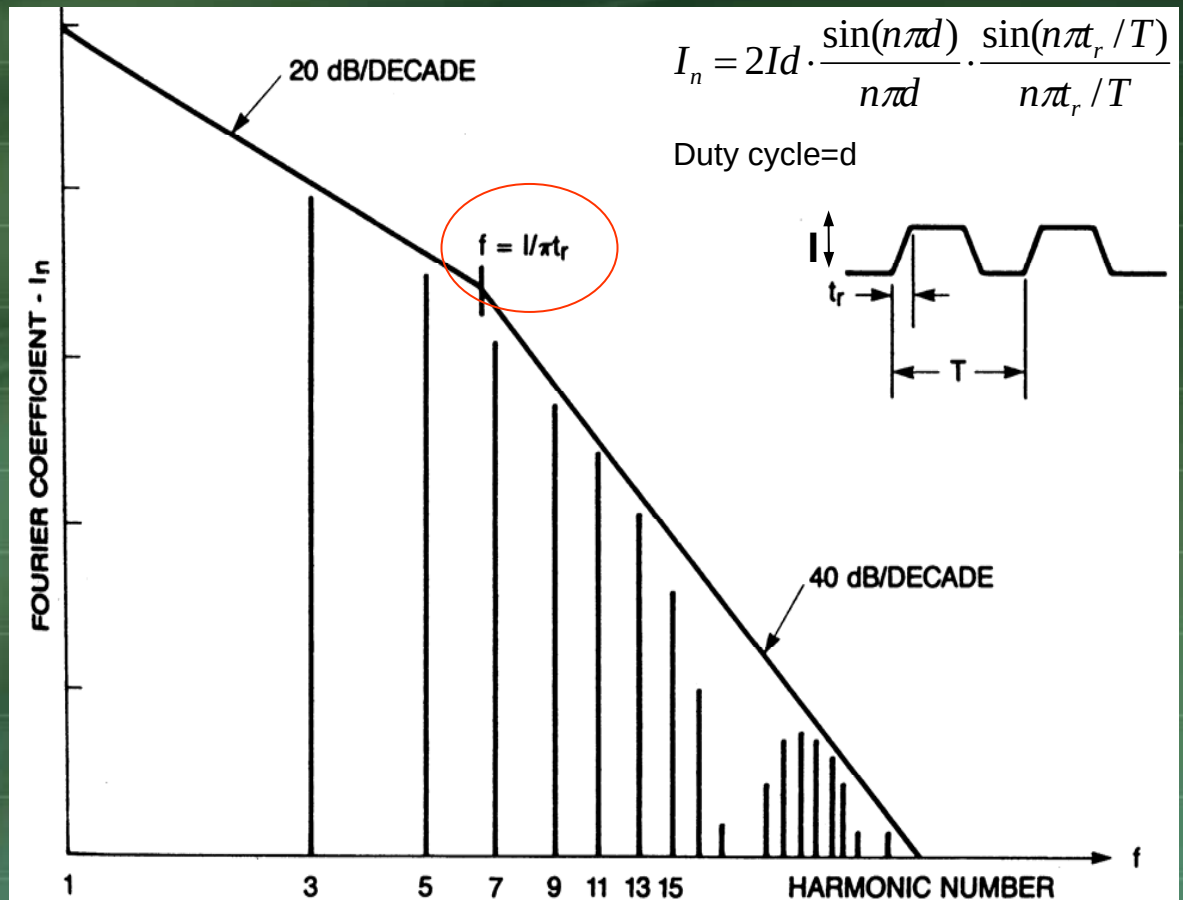
- A low inductance ground system
  - A ground plane or ground grid is best
  - Low impedance in a ground lead
- A source of charge (a capacitor) *near* each logic gate



- *All unused inputs must be connected somewhere, and not floating. It is especially important for CMOS because of its high input impedance.*

Frequency Domain

- Which is the point beyond that the energy content in harmonics can be negligible ?



Ground Bus Noise

- The power-supply transients can be controlled by proper use of decoupling capacitors, *but the signal currents in the ground can not be decoupled or bypassed.*
- To decrease the ground noise, the impedance of the ground must be minimized
  - *For digital circuit, inductance is the most concern than resister on printed wiring board*.
    - Ground path：using *parallel paths* is a good method to provide a low-impedance lead.
    - Package effect

Ground Bus Noise

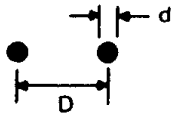
Package

IC Package	Stray capacitor	Stray inductor
DIP	0.4 ~ 1 pf	2 ~ 18 nH
PGA (Pin Grid Array)	1 pf	2 nH
SMD (Surface Mounted Package)	1pf	1 ~ 12 nH
Wire Bounding	0.5 pf	1 ~ 2 nH
TAB	0.6 pf	1 ~ 6 nH
PCB thru-hole via	1 pf	1 nH

Ground Bus Noise

- Ideally a power supply is a zero impedance source of voltage.
- They are ex3 and ex4 on the right side that have the lowest characteristic impedance.

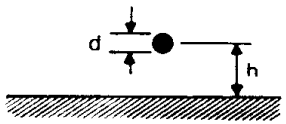
PARALLEL WIRES



$$Z_0 = \frac{120}{\sqrt{\epsilon_r}} \cosh^{-1}\left(\frac{D}{d}\right)$$

FOR $D/d \geq 3$, $Z_0 = \frac{120}{\sqrt{\epsilon_r}} \ln\left(\frac{2D}{d}\right)$

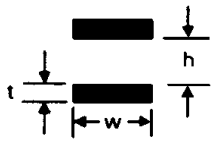
WIRE OVER GROUND



$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \cosh^{-1}\left(\frac{2h}{d}\right)$$

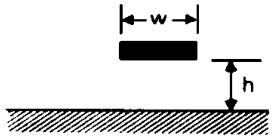
FOR $2h/d \geq 3$, $Z_0 = \frac{60}{\sqrt{\epsilon_r}} \ln\left(\frac{4h}{d}\right)$

PARALLEL FLAT CONDUCTORS



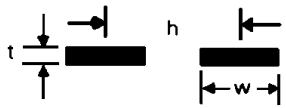
FOR $w \gg h$ and $h \gg t$, $Z_0 = \frac{377}{\sqrt{\epsilon_r}} \left(\frac{h}{w}\right)$

FLAT CONDUCTOR OVER GROUND PLANE



FOR $w \gg h$, $Z_0 = \frac{377}{\sqrt{\epsilon_r}} \left(\frac{h}{w}\right)$

FLAT CONDUCTORS SIDE BY SIDE

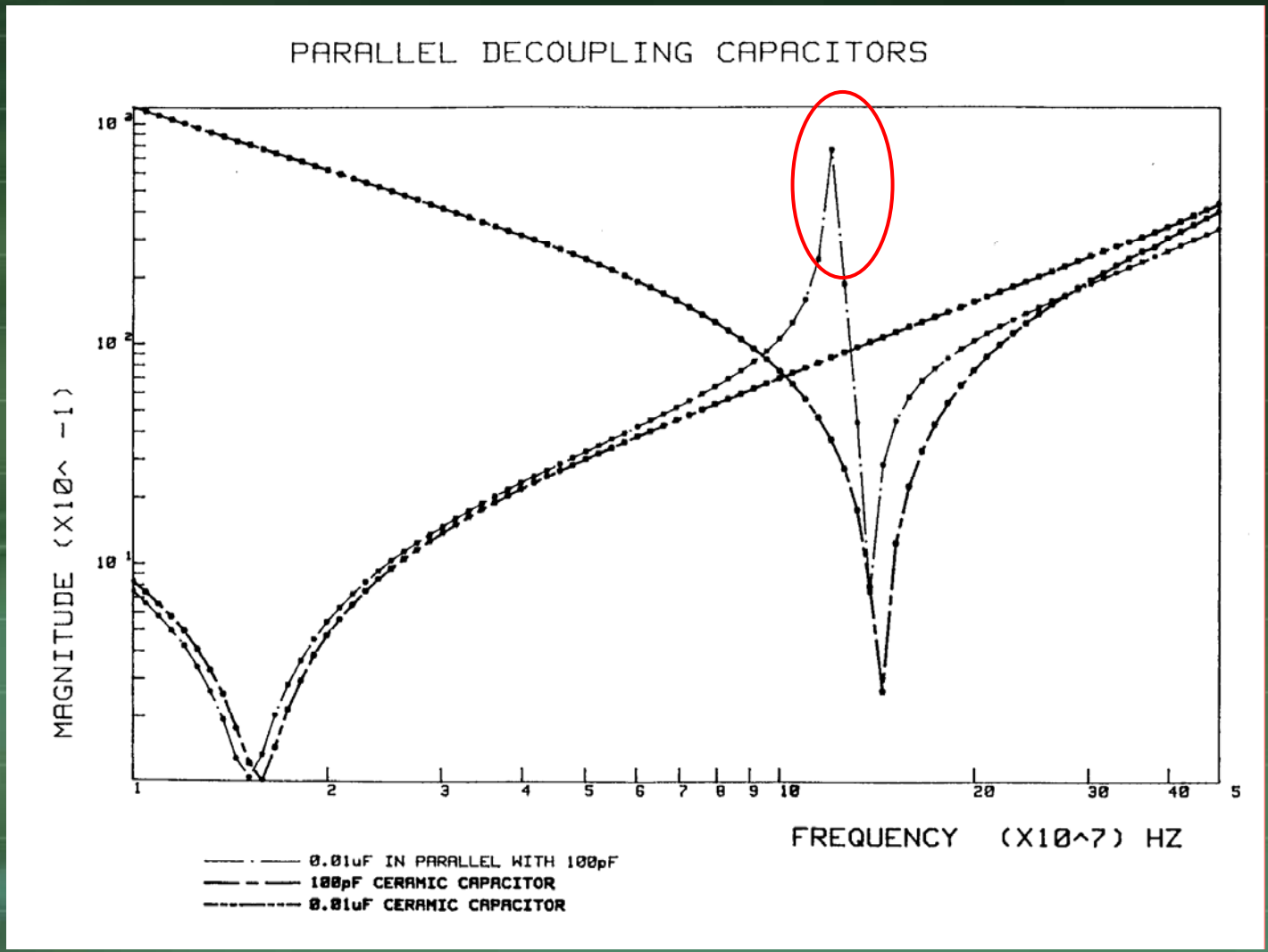


FOR $w \gg t$, $Z_0 = \frac{120}{\sqrt{\epsilon_r}} \ln\left(\frac{\pi(h+w)}{w+t}\right)$

Power Bus Noise

- Since power-supply noise can be controlled by proper filters, a power grid distribution system is not as important as a proper ground system.
- Bulk decoupling capacitor (鉭質或金屬薄膜電容比鋁質電解電容串聯阻抗小) + high-frequency(15~150MHz) capacitor (陶瓷disk ceramic或積層電容multilayer ceramic)

Power Bus Noise



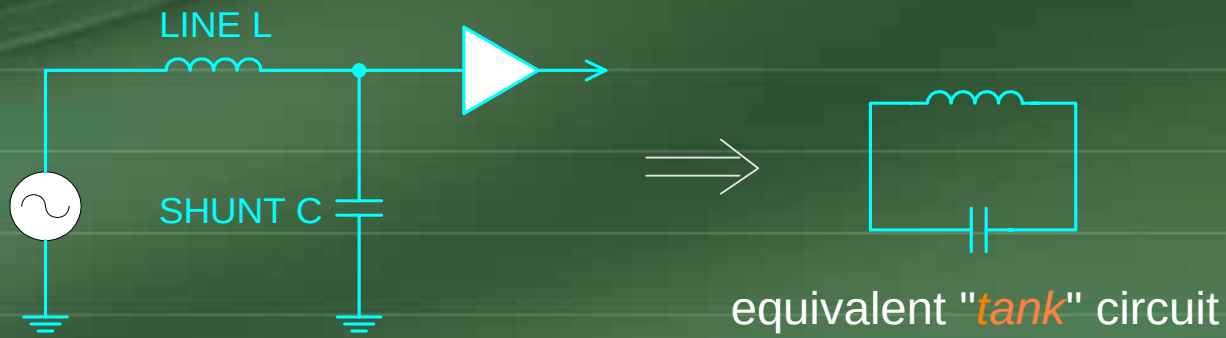
Power Bus Noise

- The filter should be as close as possible to the receptor to decrease the length of an antenna
  - To have a low impedance at high frequency, the capacitor must have a low inductance, and thus, low capacitance. A well designed PWB will already have the capacitance amount *(tens of pico.)* .
  - To determine what value of capacitor is required via the "antenna" you are dealing with. The input antenna will only be efficient if it is at least a significant fraction of a wavelength in length

$$f = 3x10^8 m / [8 \times \text{antenna length in meters}]$$

Power Bus Noise

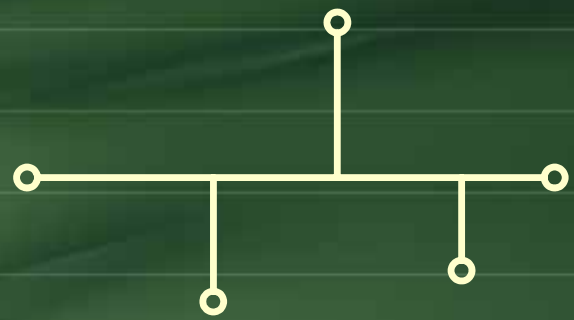
- Additional shunt capacitance or inductor will increase "*ringing*"
- Don't add extra capacitance or inductance



Reflection Strategies

Routing Topology

- Tree -- the worst way



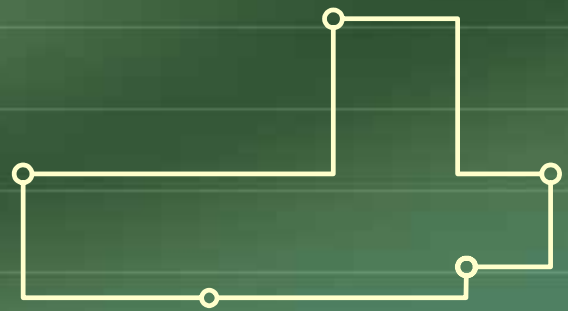
- Daisy-Chain – While with parallel terminations, it is a better way *via no branches*

Reflection Strategies

Routing Topology

- Star – While with series terminations and high drive current, it is a good way

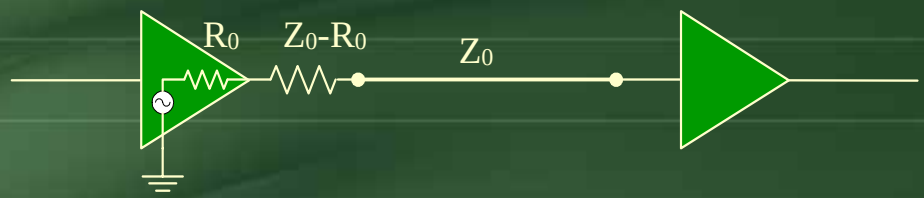
- Loop – it is bad to CM rejection via loop area



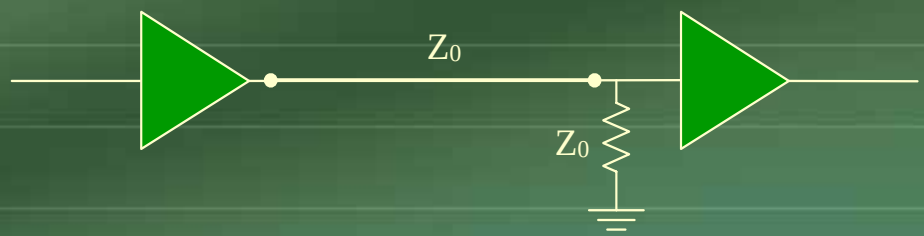
Reflection Strategies

Terminations

- Series termination resistor



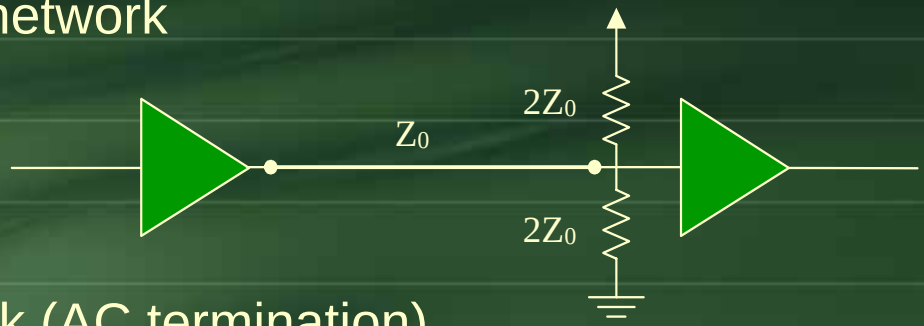
- Parallel termination resistor



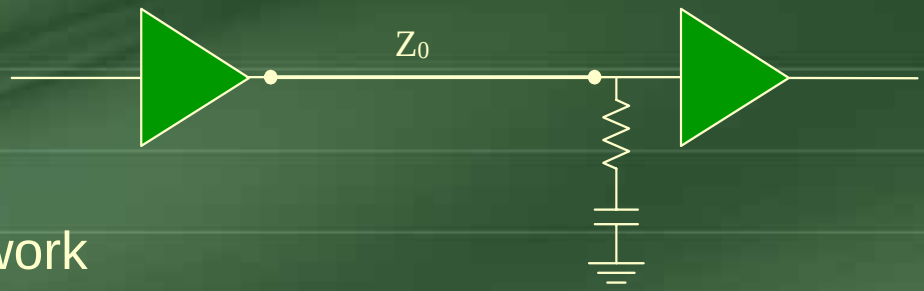
Reflection Strategies

Terminations

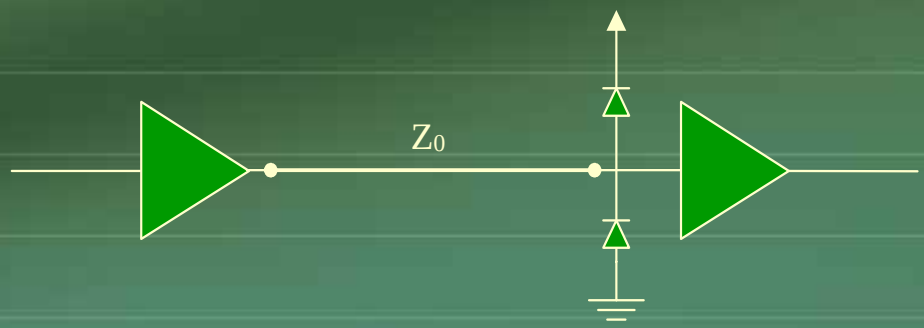
- Thevenin network



- RC network (AC termination)



- Diode network

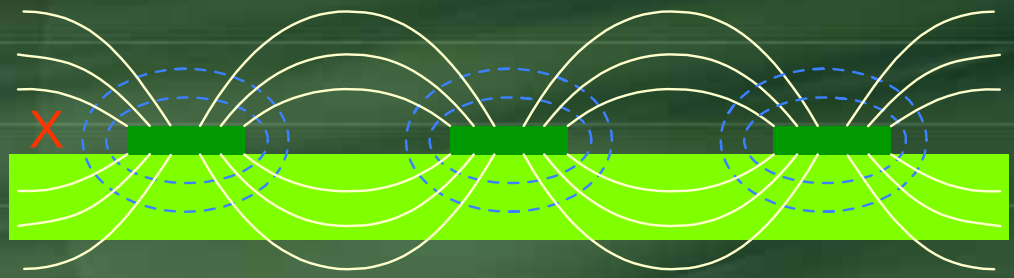


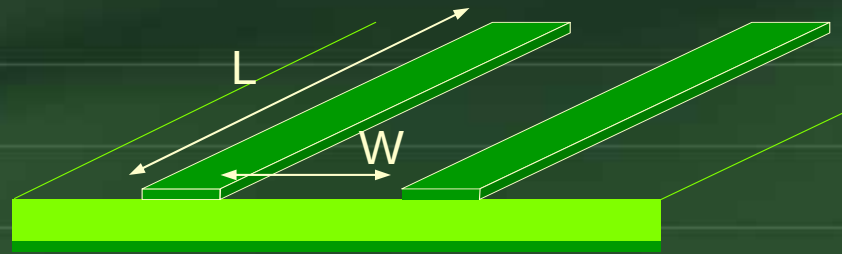
Reflection Strategies

Terminations

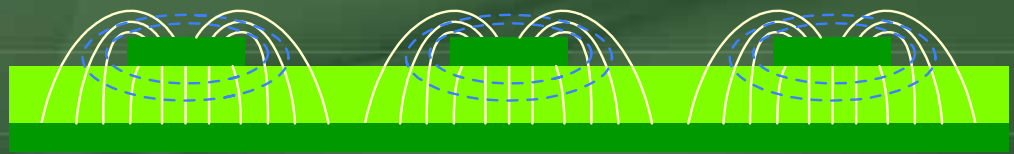
	Series	Parallel	Thevenin	RC	Diode
Application	CMOS, ECL,FACT	ECL	TTL,ECL,FACT	FACT	TTL
R value	$Z_0 - R_0$	Z_0	$2Z_0$	Z_0	--
Power consumption	low	high	high	medium	low
Drive ability	low	high	high	--	--
Propagation delay	increase	--	--	--	
Rising time	--	--	--	increase	
Design for	2nd reflection	1st reflection	1st reflection	1st reflection	both

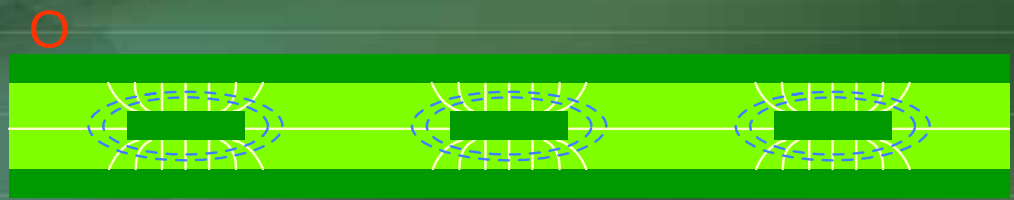
Crosstalk





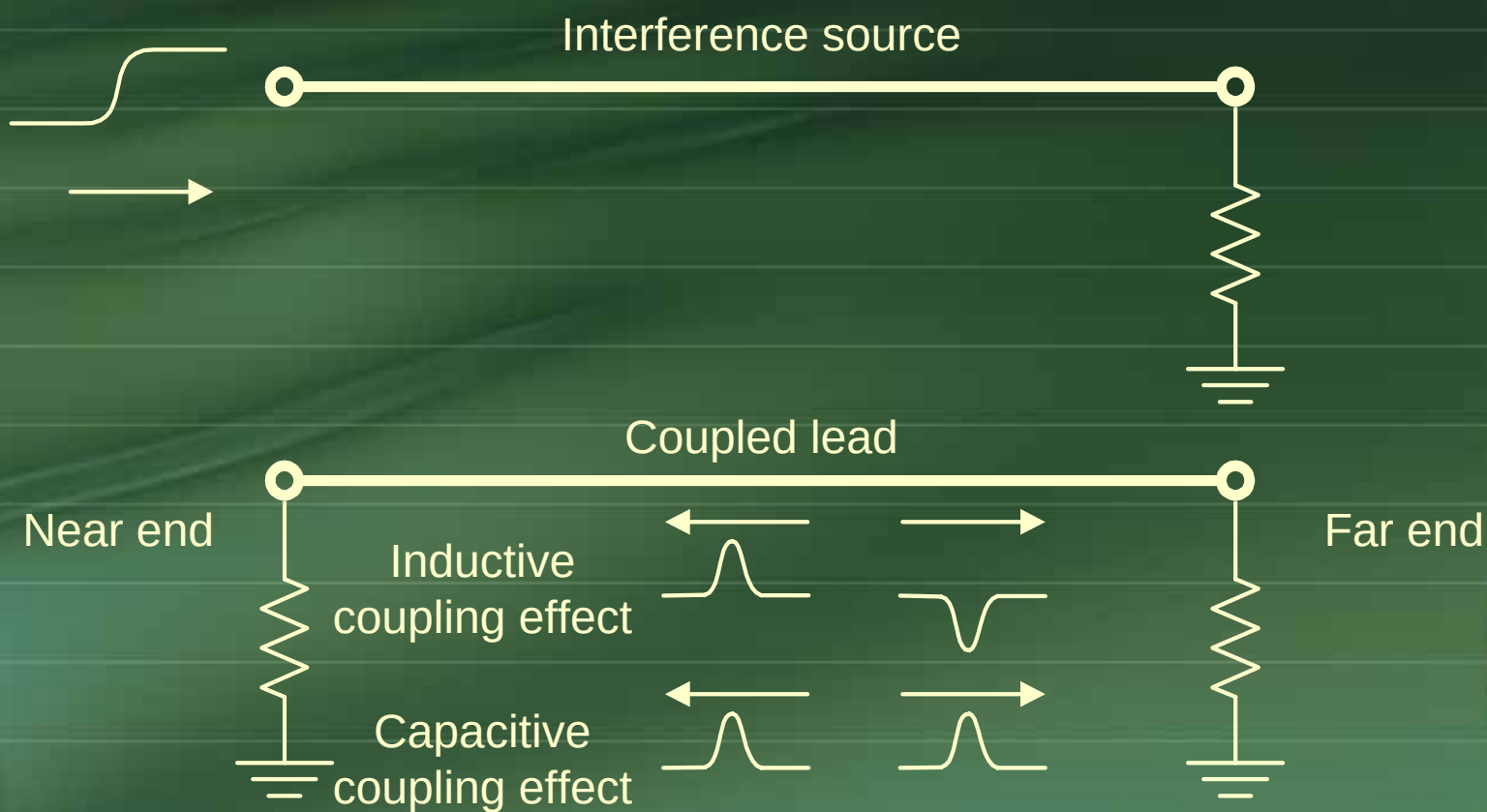
Reduce mutual inductance and mutual capacitance.





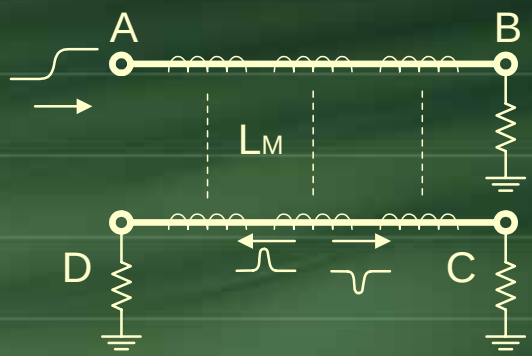
Crosstalk

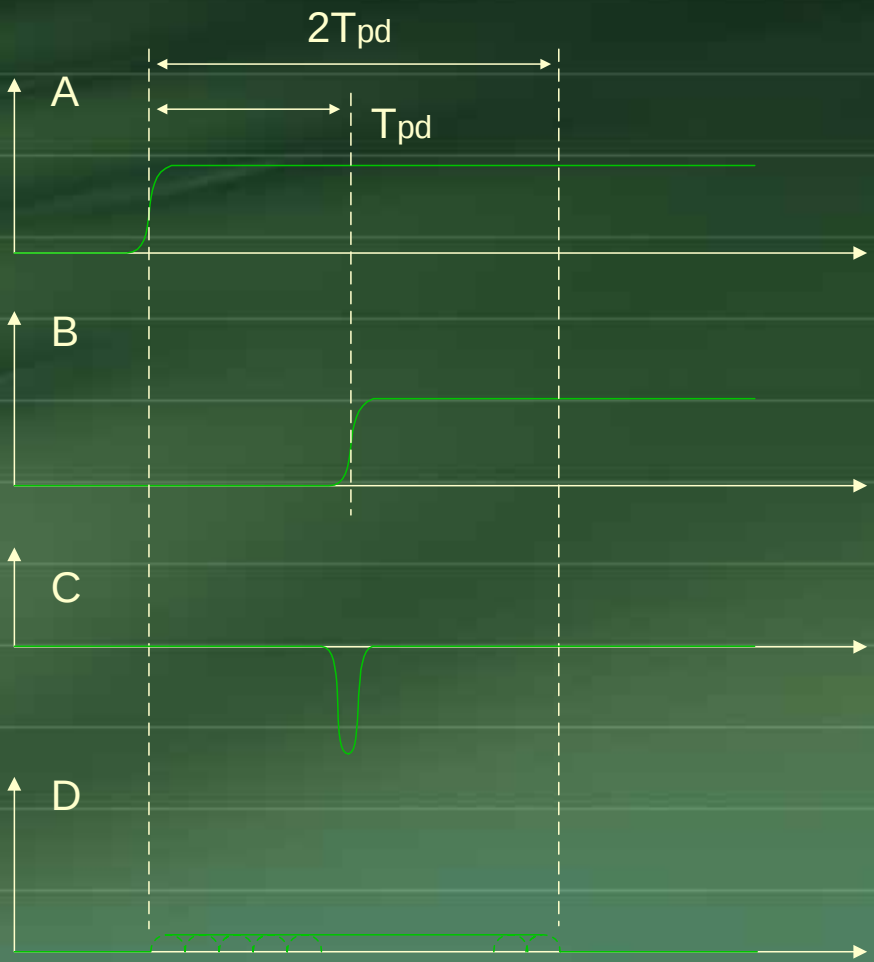
Typical Crosstalk Situation



Crosstalk

Typical Crosstalk Situation



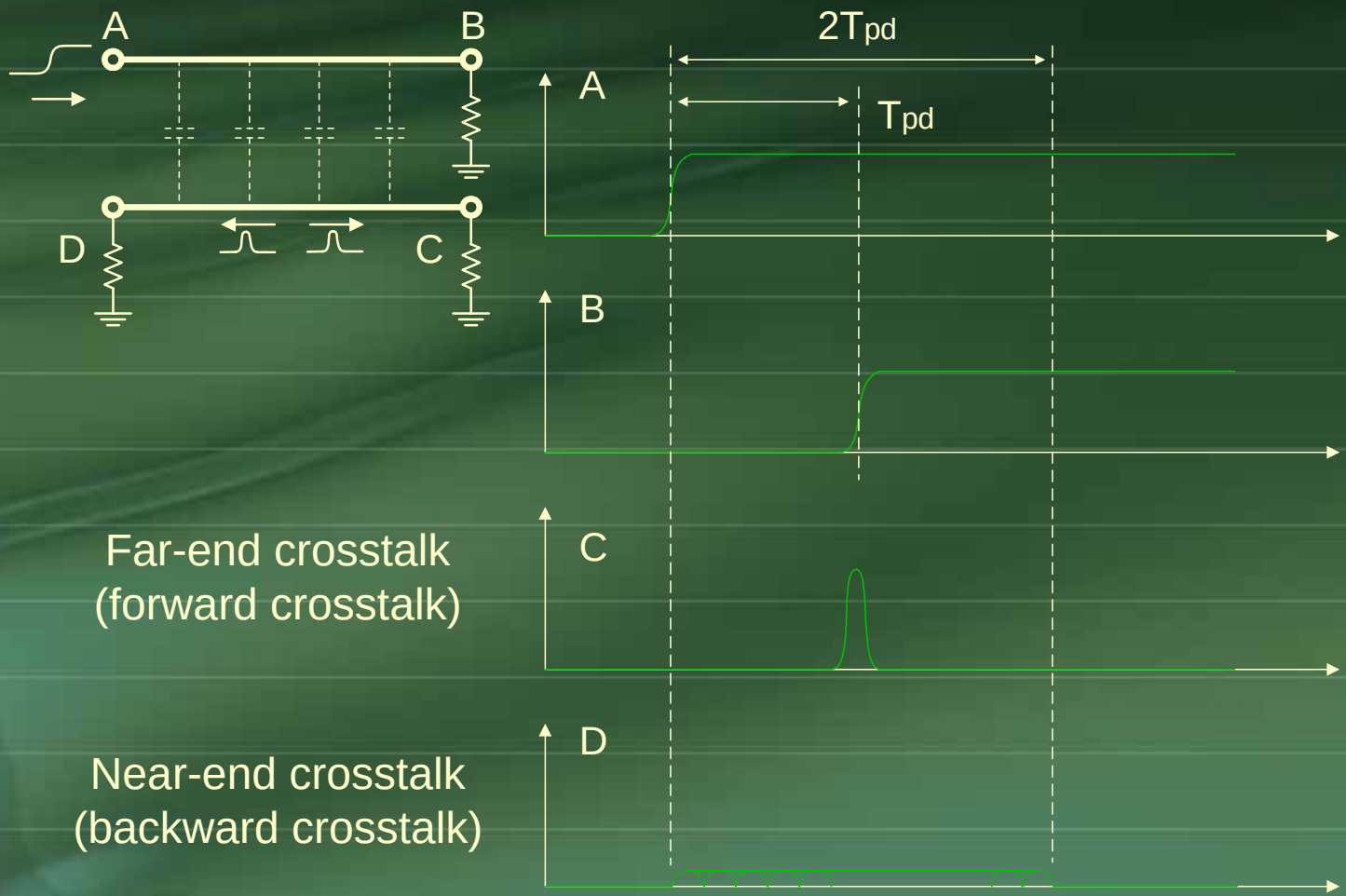


Far-end crosstalk
(forward crosstalk)

Near-end crosstalk
(backward crosstalk)

Crosstalk

Typical Crosstalk Situation

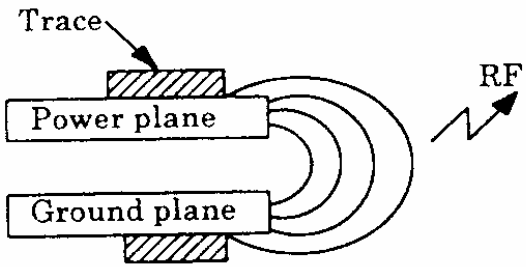


Far-end crosstalk
(forward crosstalk)

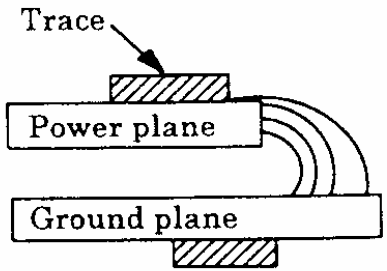
Near-end crosstalk
(backward crosstalk)

PCB Technologies

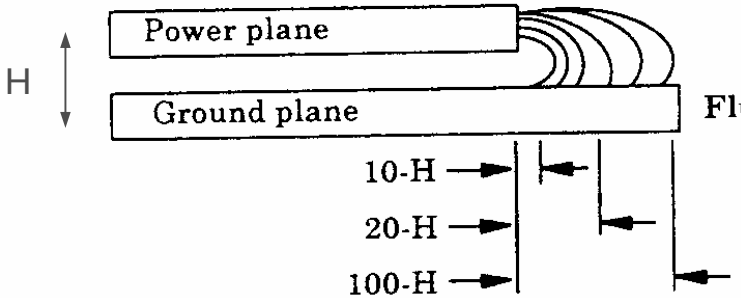
20-H rule



RF currents fringing between the power and ground planes at the edge of the board.
RF emissions occur.



RF currents do not fring from edge of board. RF currents have a return plane to couple to.
RF emissions do not occur.

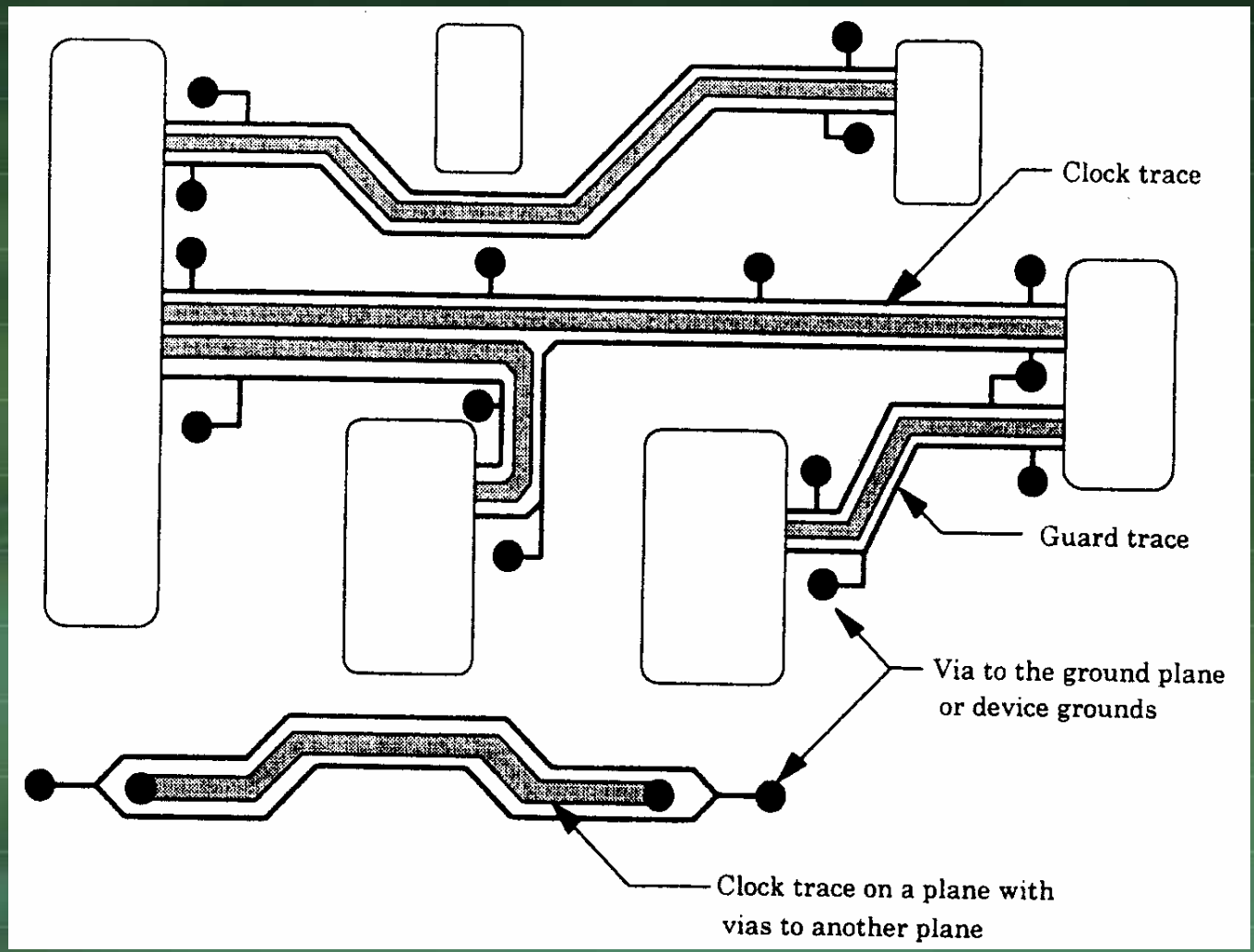


Flux Boundary Display

At 10-H, impedance change of the planes is first observed
At 20-H, we reach the 70% flux boundary
At 100-H, we approach th 98% flux boundary

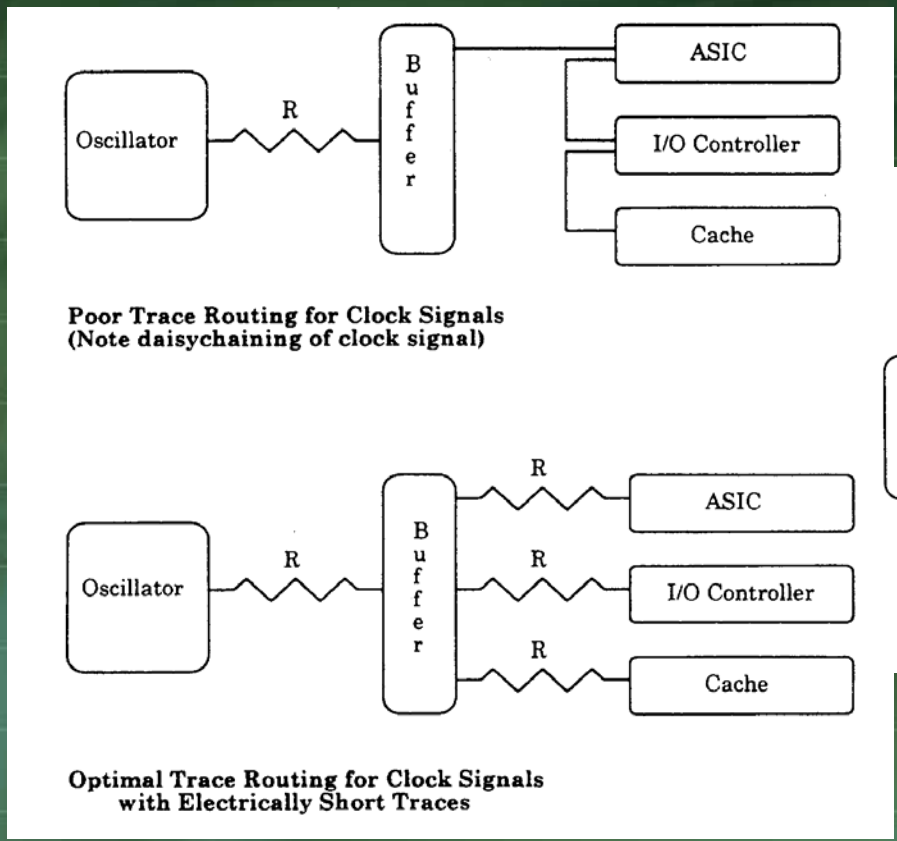
PCB Technologies

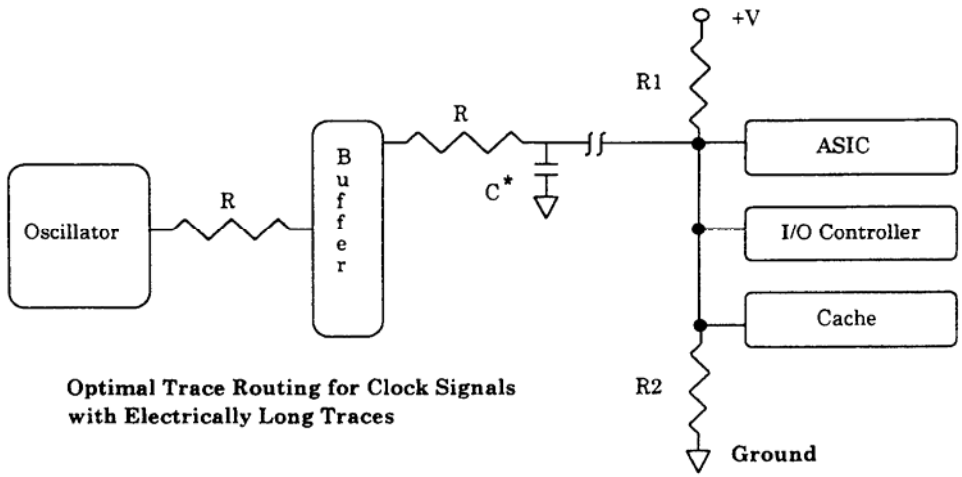
Clock trace -- using guard trace



PCB Technologies

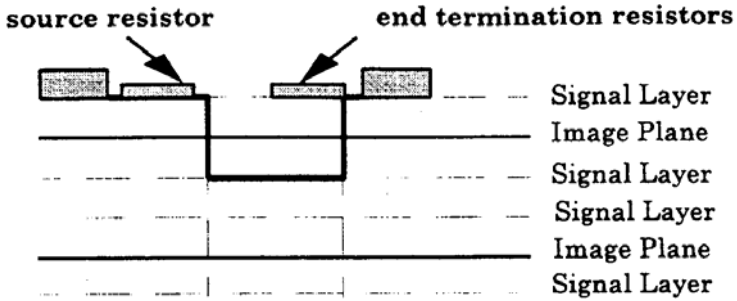
Clock trace



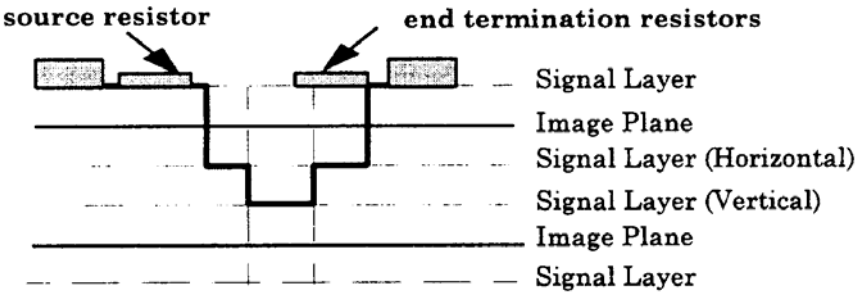


PCB Technologies

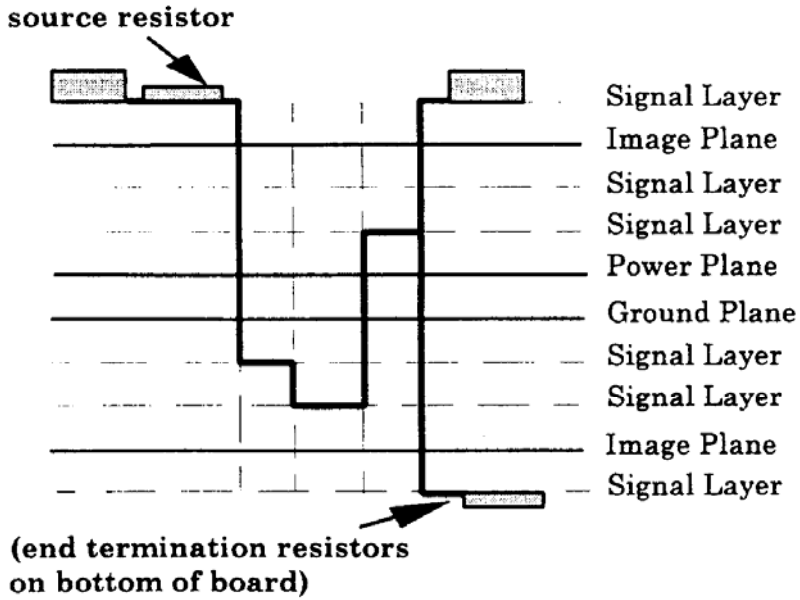
Clock trace



Best Way to Route Clock Traces Stripline
(total of 2 vias)
The perpendicular traces compliment each other



Acceptable Way to Route Clock Traces Stripline
(total of 4 vias)

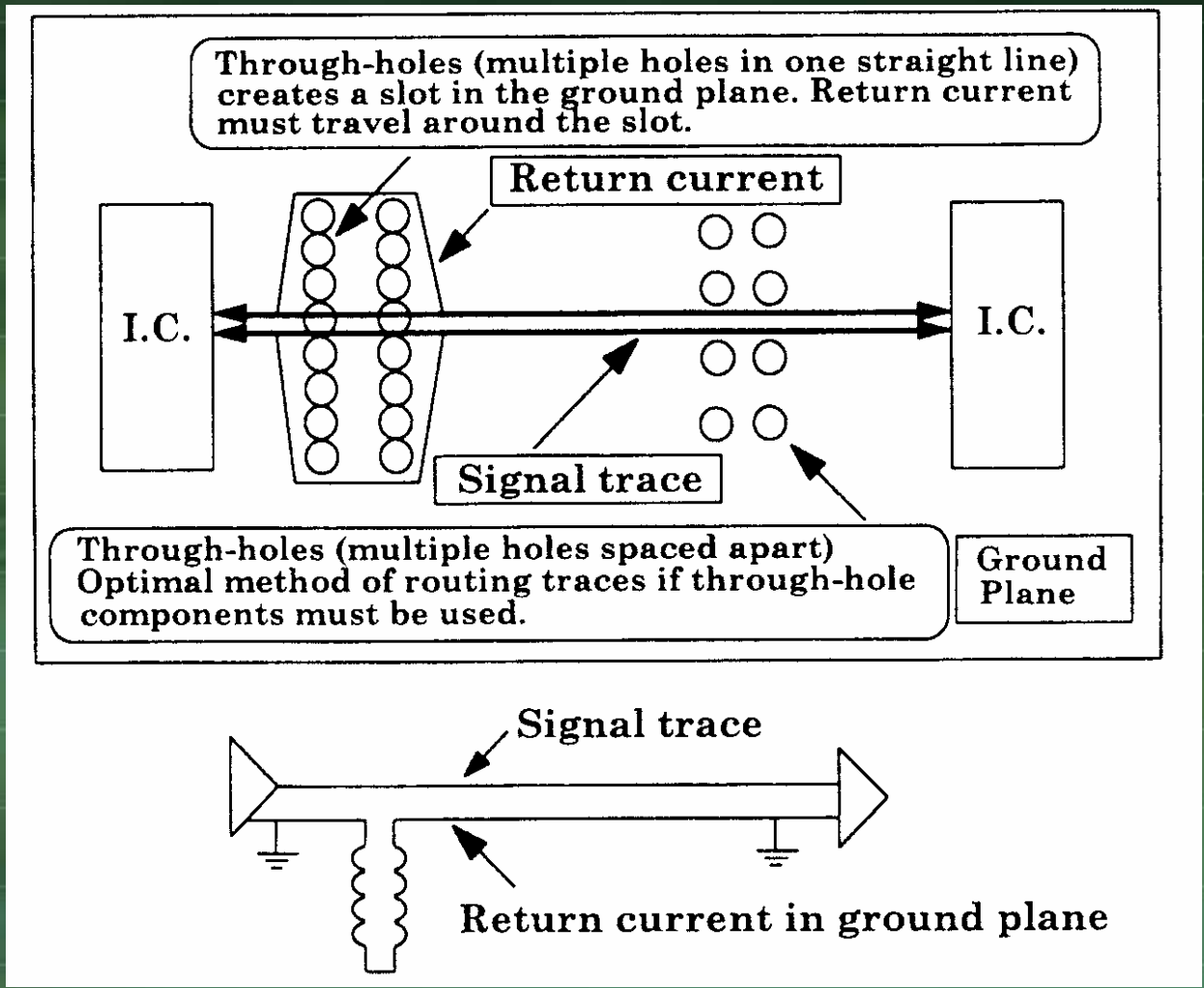


Poor Way to Route Clock Traces
(total of 4 vias)

NOTE: This method maximizes use of vias and layer jumping, both of which must be minimized.

PCB Technologies

Through-holes effect

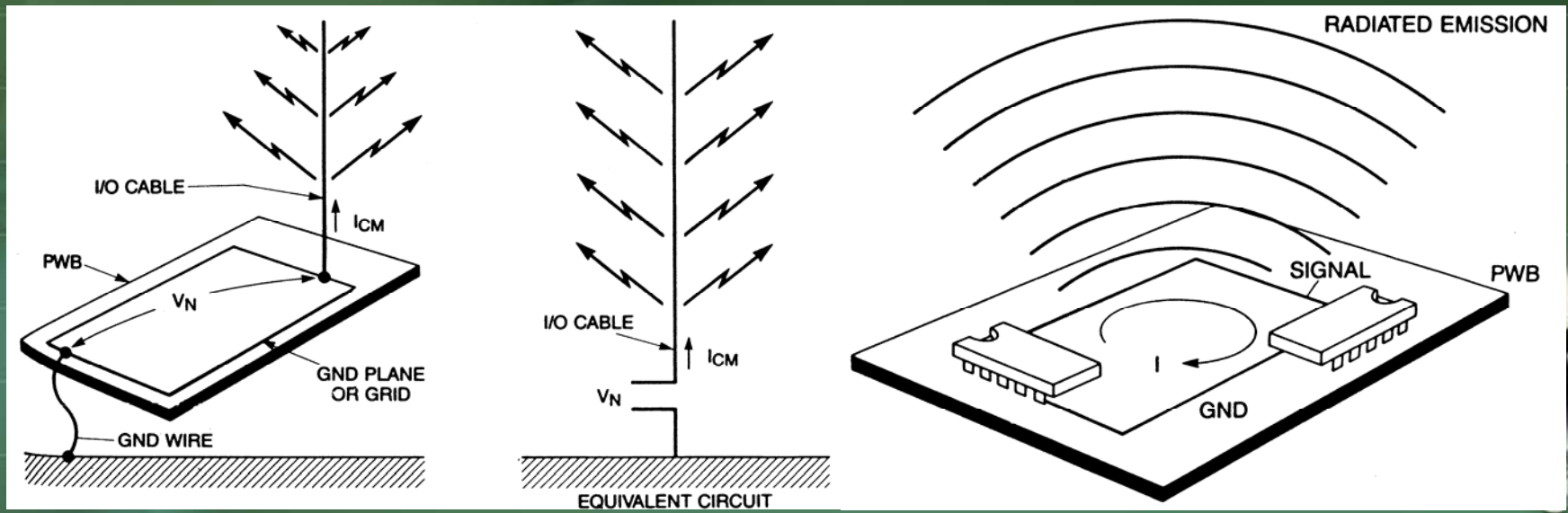


Agenda

- Digital Circuit Noise
  - Frequency Domain
  - Ground Bus Noise
  - Power Bus Noise
  - Reflection Strategies
  - Crosstalk
  - PCB Technologies
- *Digital Circuit Radiation*
  - Differential-Mode Radiation
  - Controlling DM Radiation
  - Common-Mode Radiation
  - Controlling CM Radiation

Digital Circuit Radiation

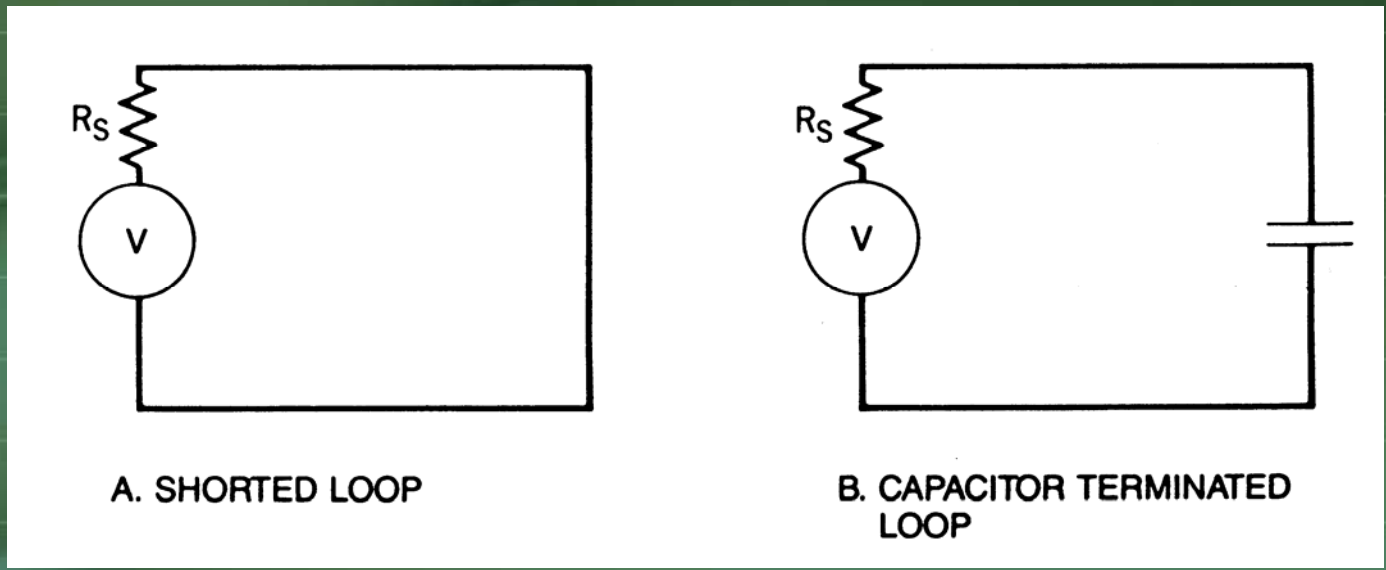
- CM radiation
  - A low current and high voltage source, like a rod or straight antenna.
- DM radiation
  - A high current and low voltage source, like a loop antenna.



Differential-Mode Radiation

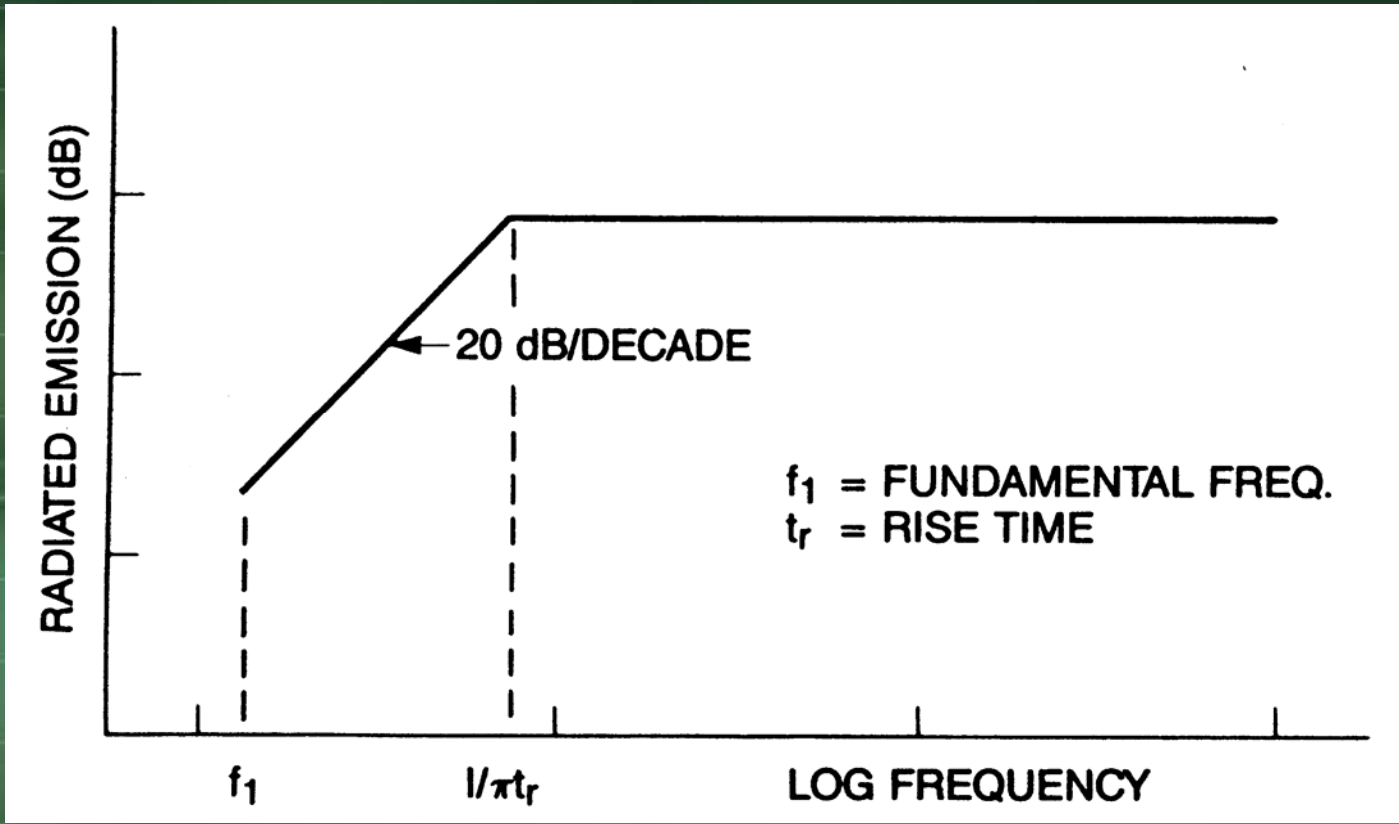
Loop Current

- The current depends on the source impedance of the circuit that drives the loop, and the load impedance of the circuit that terminates the loop.



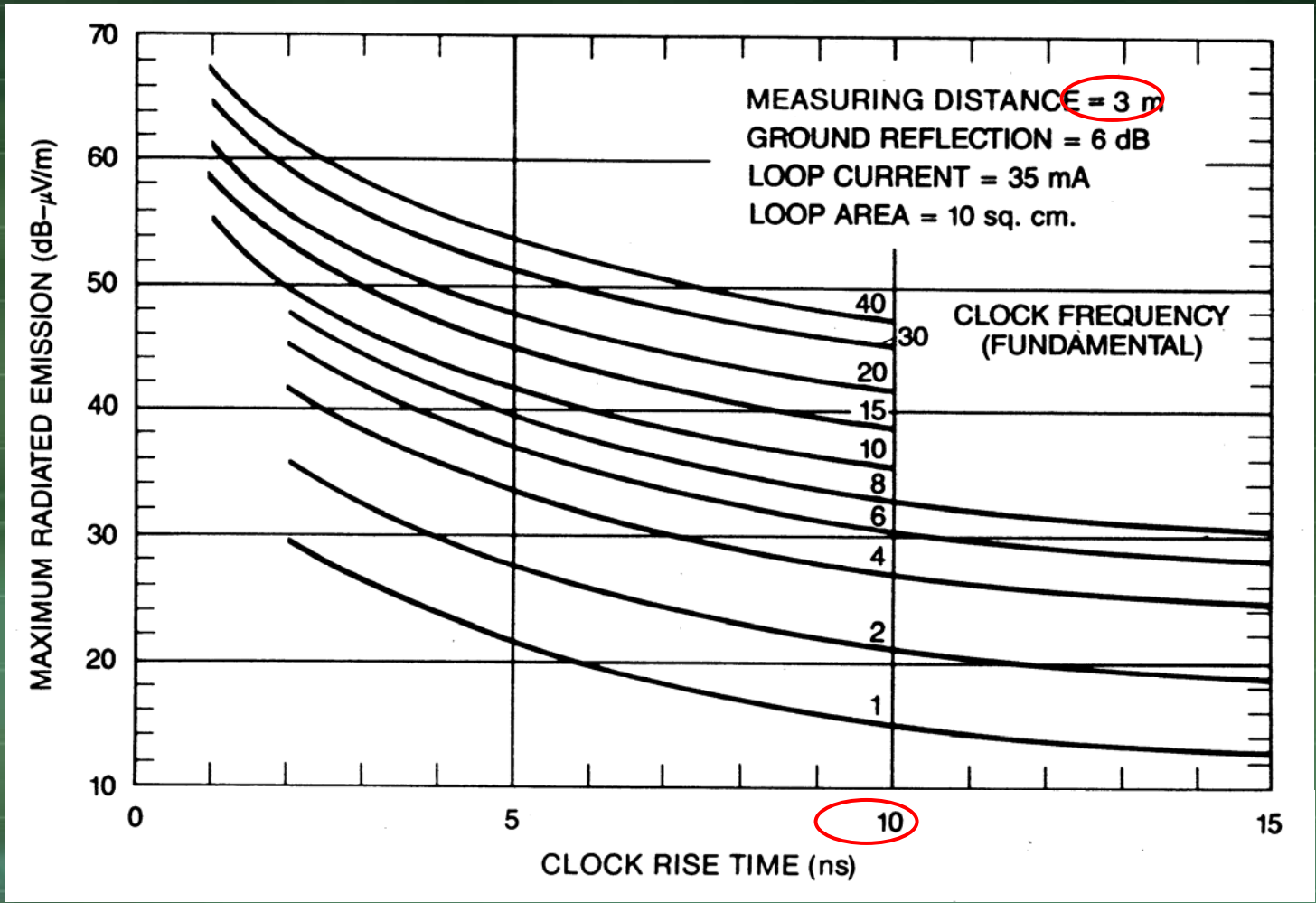
Differential-Mode Radiation

Radiated Emission Envelope



Differential-Mode Radiation

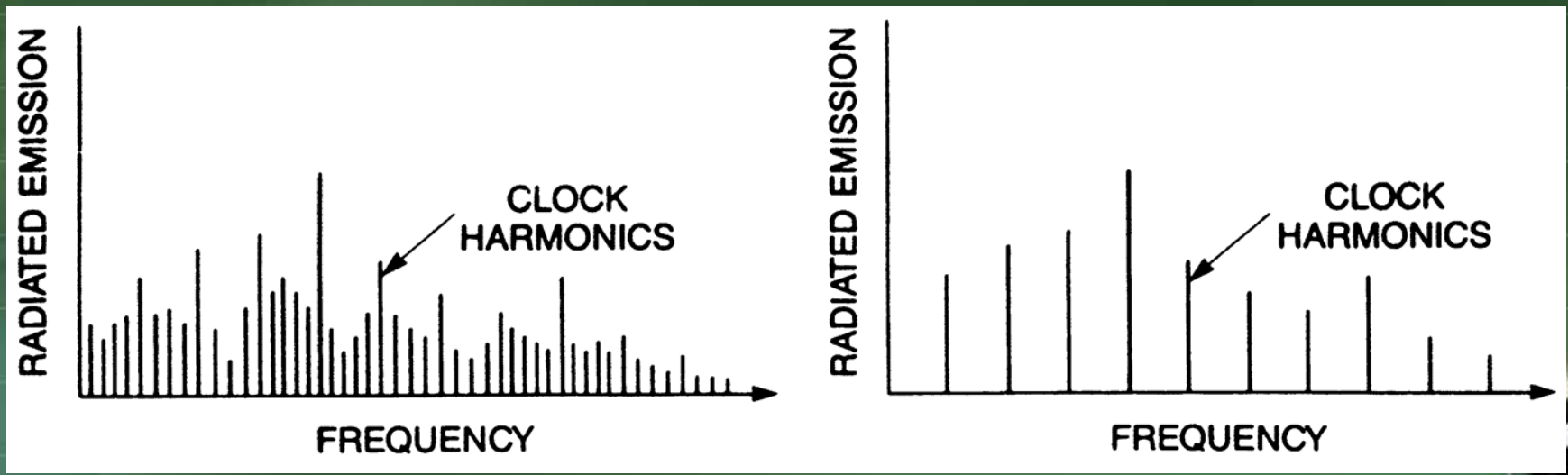
Max. Radiated Emission with Clock Frequency



Controlling DM Radiation

Board Layout

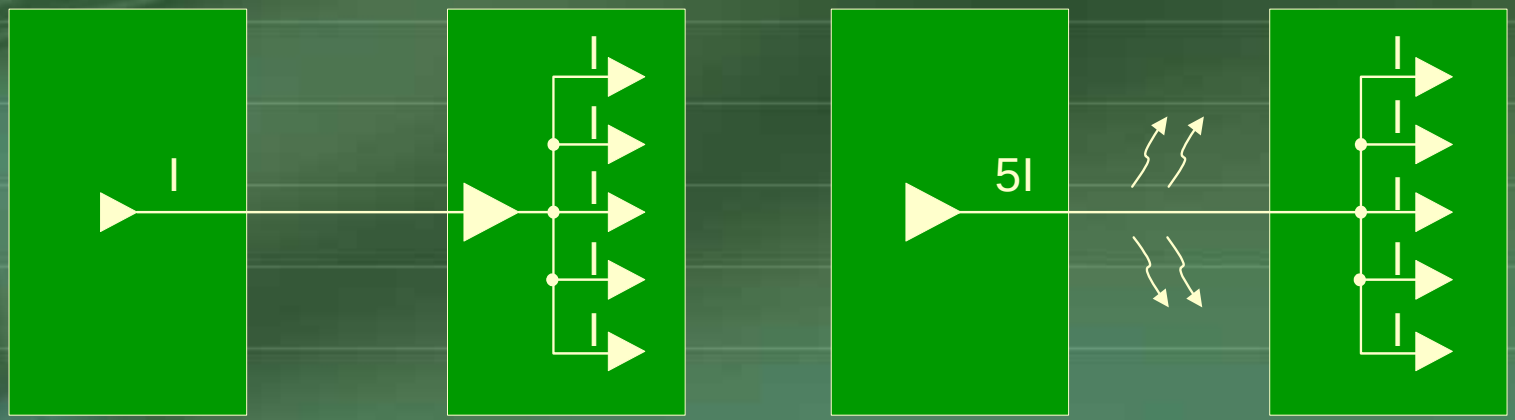
1. Minimize the loop areas formed by the signal paths.
   - *The most critical loops are those carrying the system clock.*



Controlling DM Radiation

Board Layout

2. To prevent the clock from coupling to other critical parts in a circuitry, it should be located away from the critical part and should not run parallel to critical leads for long distance.
3. Line and bus drivers may also be offenders if they carry high currents. The drivers should be close to the lines they drive.



Controlling DM Radiation

Board Layout

4. At least one signal return lead adjacent to each group of eight data or address leads is provided.
   - Using a ground grid or plane is better than a ground lead.

All conductors use just a signal ground return.
The current loop and cross-talk will be worse.

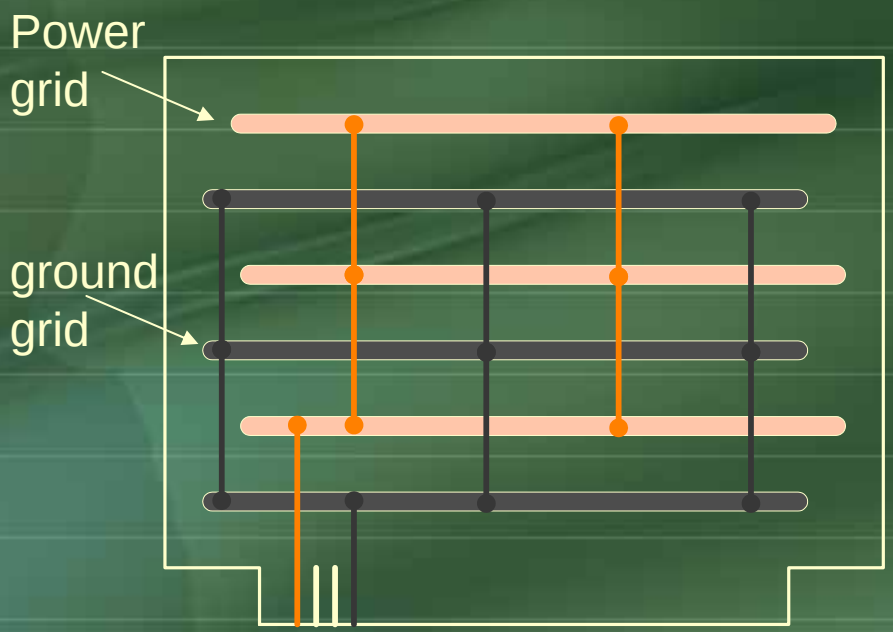
All conductors use a signal ground plane across the width of the cable, so the loop area is very small.

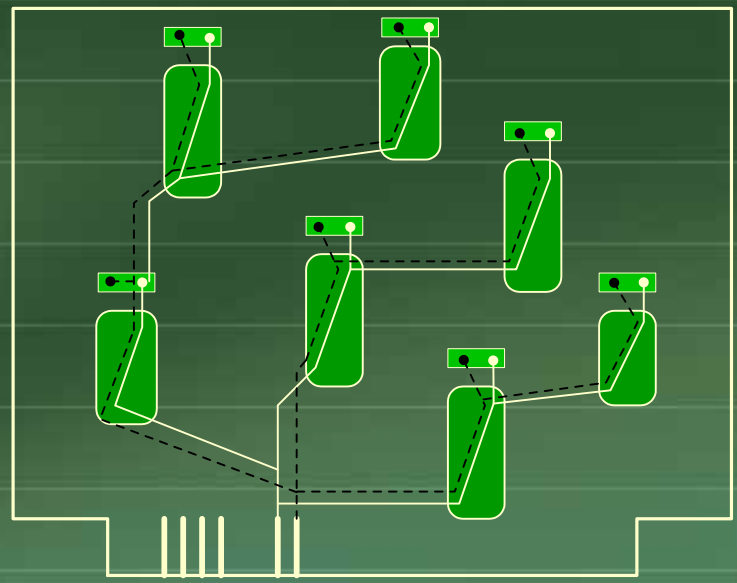
- Ground
- Signal line

Controlling DM Radiation

Board Layout

5. Loop area of the transient power-supply current during logic IC switching can be controlled by decoupling capacitors placed next to each IC -- located physically as close as possible to IC.





I/O power

Commonly used at less than 10kHz

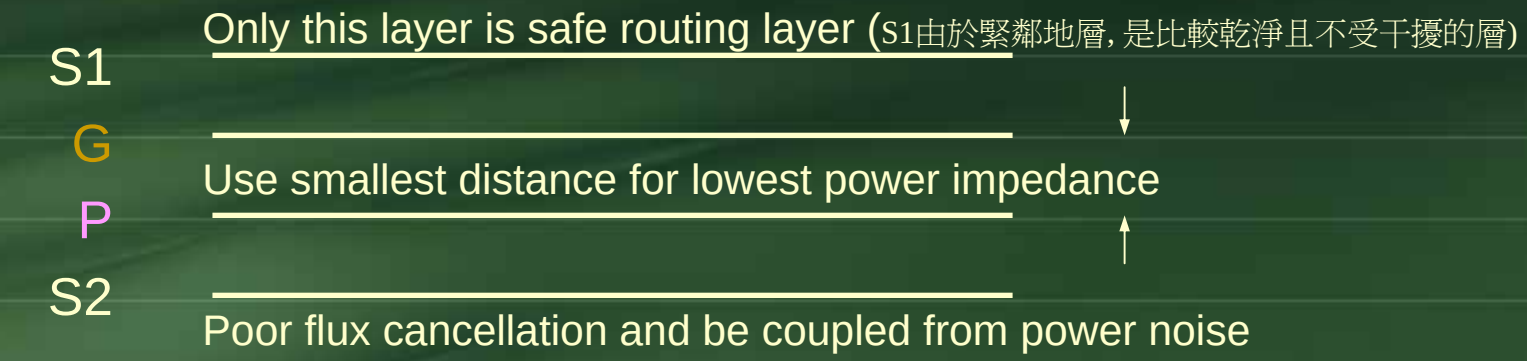
Controlling DM Radiation

Multilayer Boards – Stackup(堆疊) Assignment

Layer #	1	2	3	4	5	6	7	8	9	10	*Comments*
2 layers	S1(**G**)	S2(**P**)									Just for lower-speed designs
4 layers (2 routing)	S1	**G**	**P**	S2							Default critical signals to S1 only
6 layers (4 routing)	S1	**G**	S2	S3	**P**	S4					Just for lower-speed designs
6 layers (4 routing)	S1	S2	**G**	**P**	S3	S4					Default critical signals to S2 only
6 layers (3 routing)	S1	**G**	S2	**P**	**G**	S3					Default high-speed signals to S2, S3
8 layers (6 routing)	S1	S2	**G**	S3	S4	**P**	S5	S6			Default high-speed signals to S2, S3
8 layers (4 routing)	S1	**G**	S2	**G**	**P**	S3	**G**	S4			Best for EMC
10 layers (6 routing)	S1	**G**	S2	S3	**G**	**P**	S4	S5	**G**	S6	Best for EMC, but R4 is susceptible to power noise .

Controlling DM Radiation

Multilayer Boards – Stackup Assignment



- Each and every routing layer must be adjacent to a solid plane(power or ground).
- The more numbers of ground layers (G) exist, the better EMC performance will be. 成本可以接受的情況下, 越多的地層越好, 因爲可以讓相鄰的訊號層有最小的訊號迴路阻抗, 並且減少EMI
- The power layer (P) can be considered as a noisy layer.
  - *High-speed clock traces are routed adjacent to a ground plane and not to the power plane.* 高速訊號放S1可以獲得最小的走線電感 , 因爲訊號下方直接有return path的地
  - *A power layer should be beside a ground layer to get better performance.* 電源層與地層一定要緊鄰 , 以獲得最大的寄生電容於其間 , 並且得到最小的電源迴路面積與電源迴路阻抗

Controlling DM Radiation

Multilayer Boards – Stackup Assignment

- High density、low cost but *worse performance*
  - High density : 4 layer for signal routing
  - Worse performance : power is far from ground layer
  - S1、S2 are better layers for high-speed signals
  - S3、S4 are dirtier layer

Controlling DM Radiation

Multilayer Boards – Stackup Assignment

- High density、low cost and middle performance
  - High density : 4 layer for signal routing
  - Middle performance : power is adjacent to ground layer
  - S2 is the best layers for high-speed signals, and S3 is the dirtiest layer
  - Signals on S1、S4 will be serious EMI emission lines

Controlling DM Radiation

Multilayer Boards – Stackup Assignment

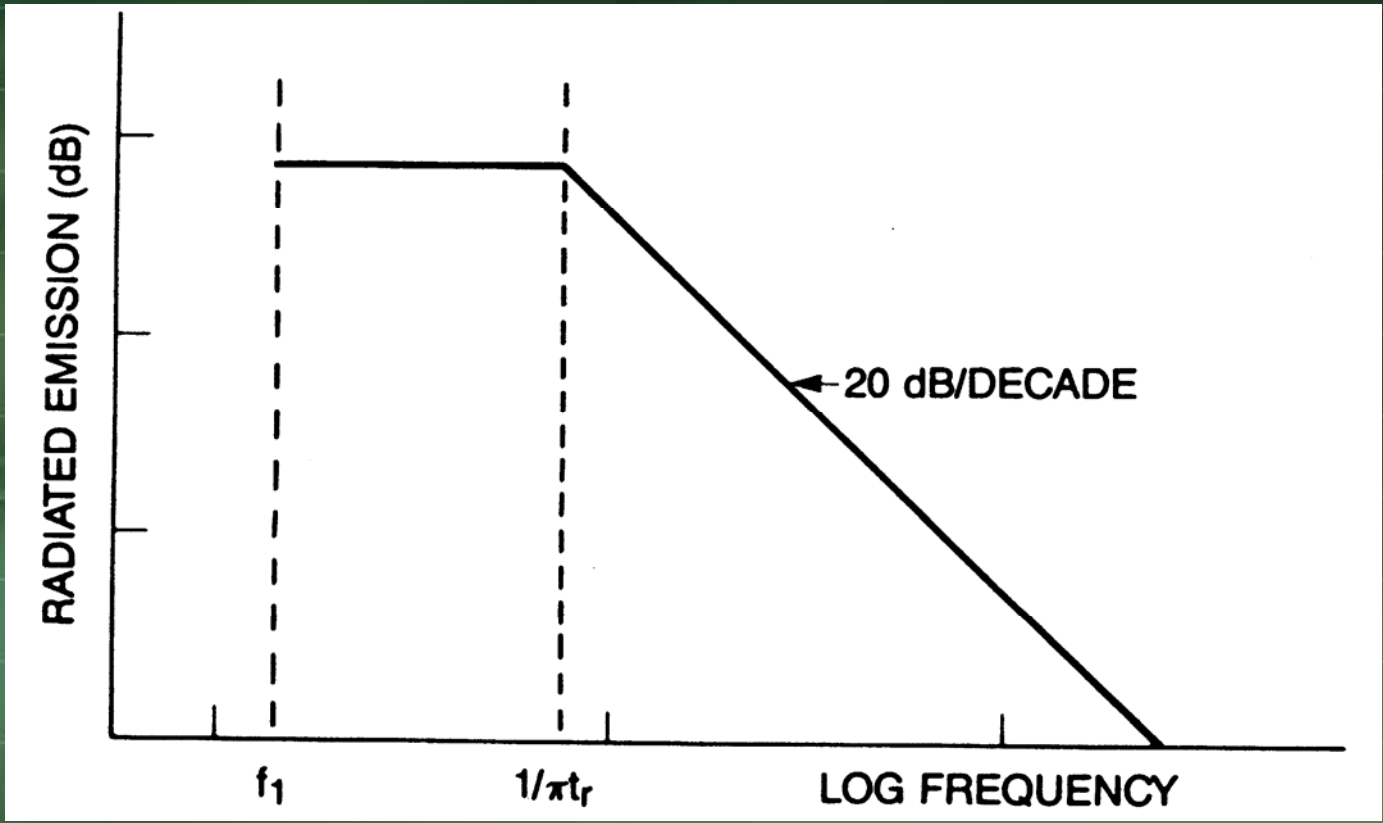
- Middle density but good performance
  - Middle density : 3 layer for signal routing
  - *Good performance* : power is adjacent to ground layer
  - *S1、S2、S3 are all good layers for high-speed signals*

Common-Mode Radiation

- CM radiation is harder to control and normally determines the overall emission performance of the product. ([1] p.313)
- *It takes three orders of magnitude more DM current than CM current to produce the same field.* That is, a CM current of a few micro-amperes can cause the same amount of radiated emission as a few milliamperes of DM current.

Common-Mode Radiation

Radiated Emission Envelope

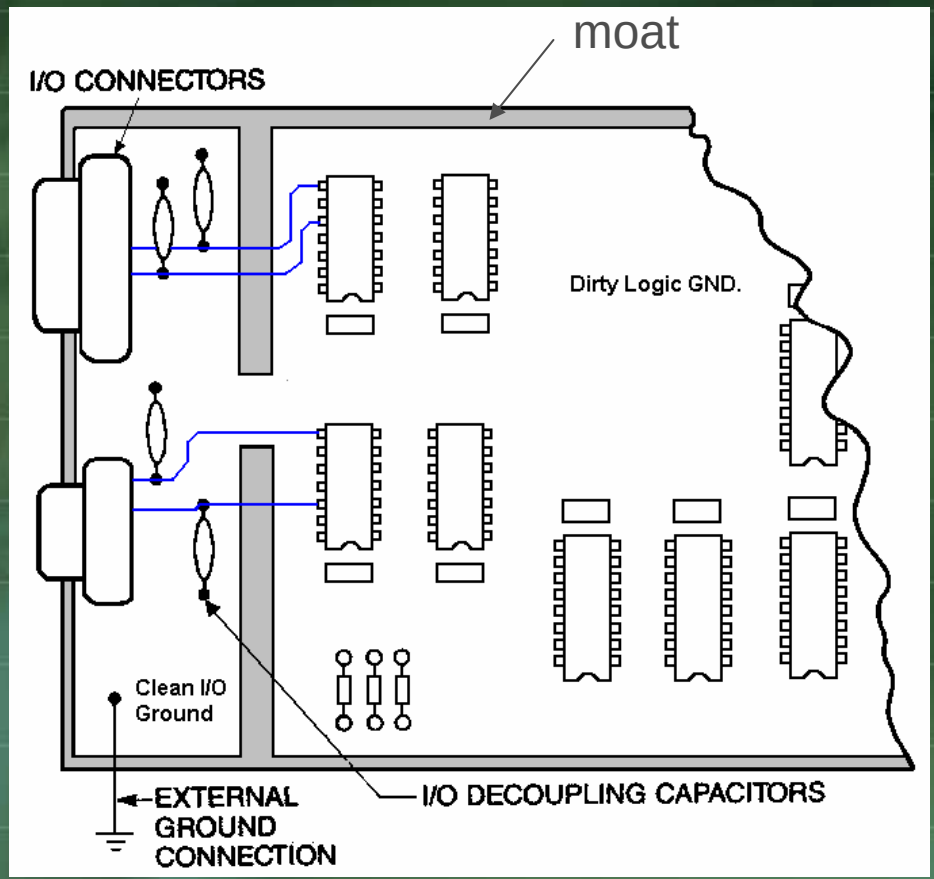


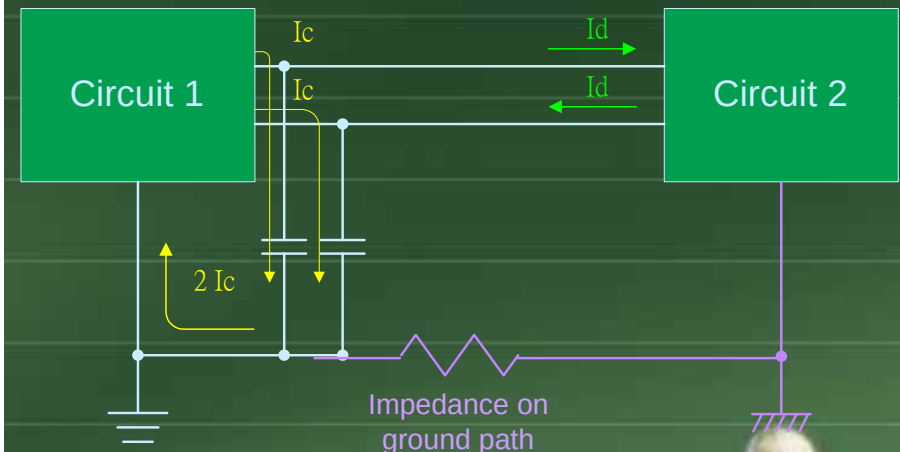
Controlling CM Radiation

- As in the case of DM radiation, it is desirable to limit both the rise time and frequency of the signal to decrease CM emission.
- CM current can be controlled by
  - Minimizing the source voltage that drives the antenna (normally the ground potential).
    - *Using a ground grid or plane*
  - Providing a large *CM impedance (choke)* in series with the cable.
  - Isolating
  - Shunting the current to ground
  - *Shielding the cable*

Controlling CM Radiation

Shunting the current to ground



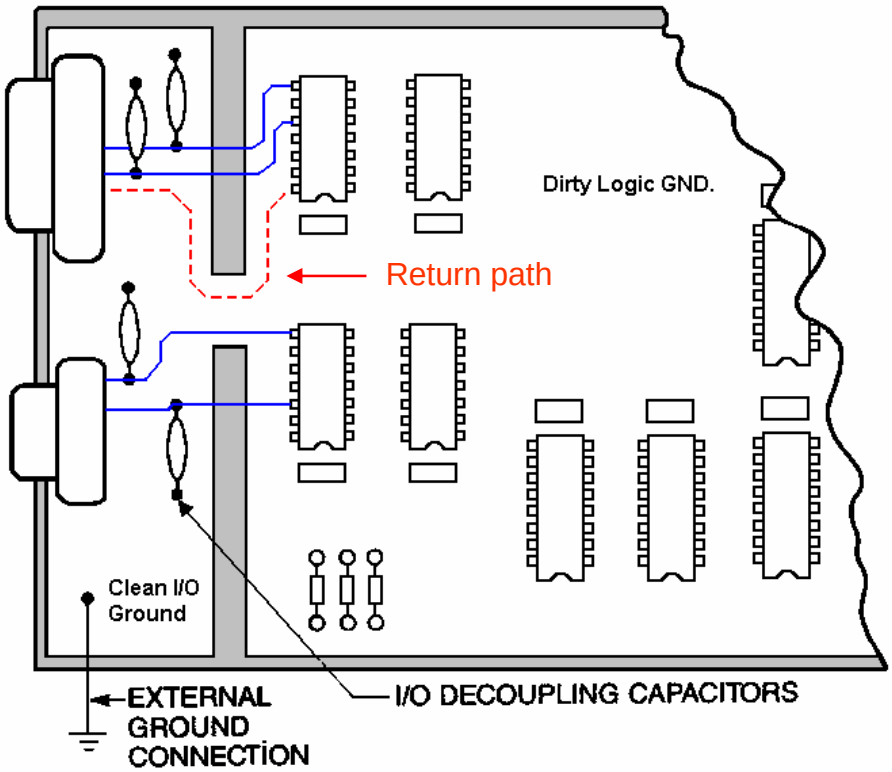


Controlling CM Radiation

Bridge in a Moat -- partitioning

X

Moat violation



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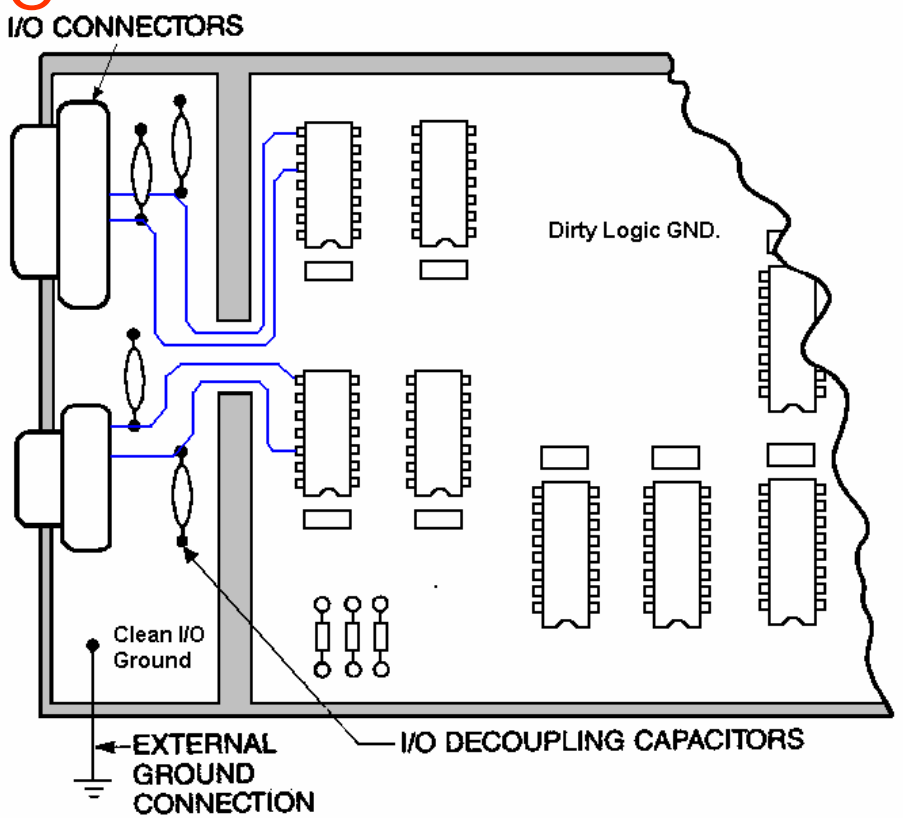

- *High-speed return currents follow the path of least inductance, not the path of least resistance.*
- *The lowest inductance return path lies directly under a signal conductor, minimizing the total loop.*

Summary

- Due to high switching speed, digital logic can be a source of radiated and conducted emission.
- Ground impedance in digital systems can be minimized by using ground plane or ground grid.
- Decoupling capacitors should be located next to each IC in the system.
- *The smallest-value decoupling capacitor that will be able to do the job is best.*
- A bulk decoupling capacitor should be used to recharge the individual IC decoupling capacitors.
- All unused inputs on digital logic gates can not be floating.
- The slowest and lowest-power logic family that can do the job should be used to minimize noise and interference.

Summary

- *All clock leads must have adjacent ground returns, and when laying out the printed wring board, they should be taken care at the first.*
- *All cables entering or leaving the system require treatment to control CM emission.*
- I/O drivers should be near the connector.
- Control CM current
  - Reduce CM voltage
  - Decoupling
  - Isolating
  - CM chokes
  - Cable shielding