Electromagnetic Compatibility (*EMC*)

Introduction about IC Immunity Testing

Agenda

- Semiconductor Immunity Test
  - ESD (圖片與部分內容取自柯明道教授網站)
    - Chip level test
      - Human Body Mode：MIL-STD 883E method 3015.7 or EIA/JESD 22-A114-A in EIA/JEDEC
      - Machine Mode：EIAJ-IC-121 method 20 or EIA/JESD 22-A115-A in EIA/JEDEC
      - Charged-Device Mode： EIA/JESD 22-A116-A in EIA/JEDEC
    - System level test
      - IEC 61000-4-2
  - Latch-up
    - Physical Origin of Latch-up
    - Latch-up Triggering
    - Latch-up Prevention
    - Latch-up Testing
      - Voltage trigger、Current trigger
      - EIA/JEDEC No. 78

ESD Testing Concept

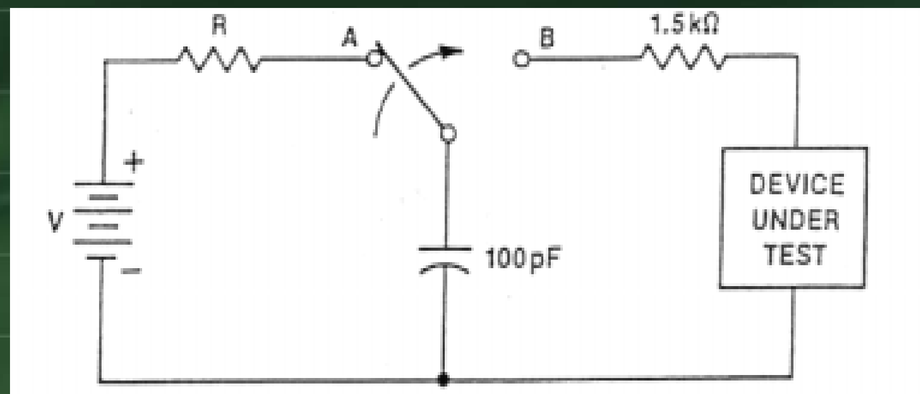
- Chip level ESD testing is just EOS issue
  - IC level design to improve ESD
- System level ESD testing includes EOS and instant huge electrical magnetic field issue
  - System level design will also effect ESD very much

Chip Level ESD Test

- ESD Mode
  - Explain what is HBM、MM、CDM
  - Compare the discharged current between these mode
- Test Method
  - Kinds of the pin combination
  - Testing process
  - Failure decision

ESD Mode

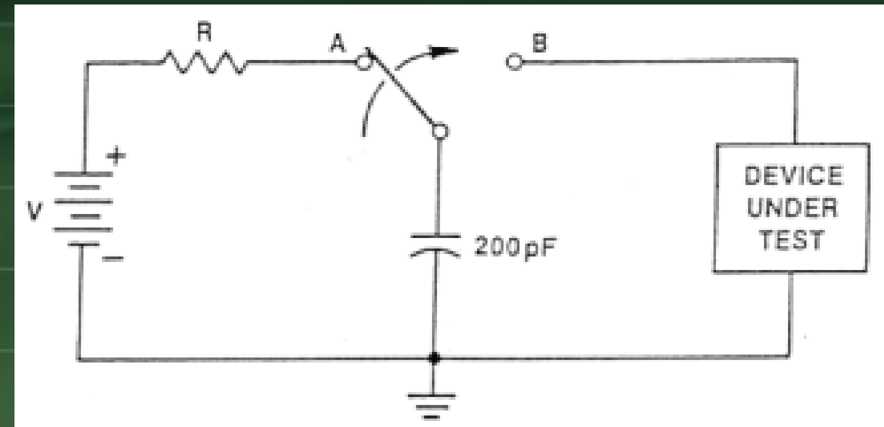
HBM：Human Body Mode



- The oldest and most commonly used model
  - 1.5K discharged resister to reduce the instant ESD current peak
- ESD Association HBM standard was recently revised
  - The number of zaps per stress level and polarity has been reduced from 3 to 1. Also, the minimum time interval between zaps has been reduced from 1s to 300ms.
  - The maximum rise time for an HBM wave form measured through a 500 ohm load was relaxed from 20 to 25ns

ESD Mode

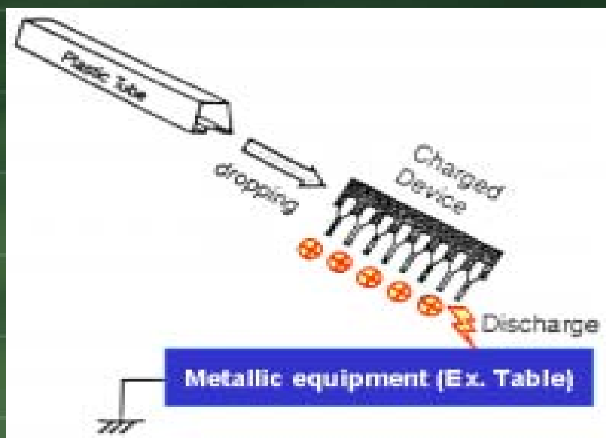
MM：Machine Mode

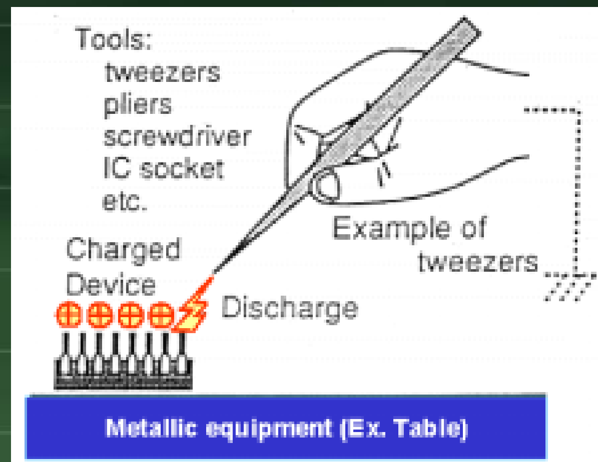


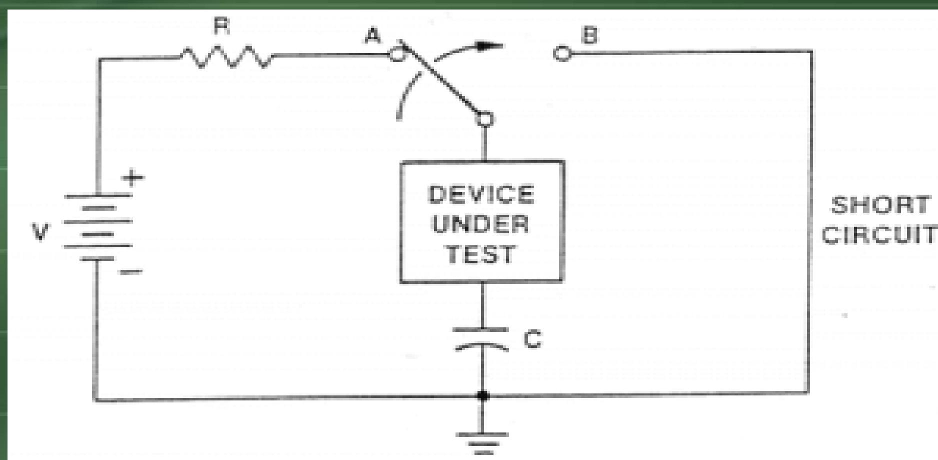
- Originating in Japan as the result of trying to create a worst-case HBM event
  - *No discharged resister (like metal), so the instant ESD current peak is very serious.*

ESD Mode

CDM：Charged-Device Mode







ESD Mode

CDM：Charged-Device Mode

1 Ohm, Current Measurement Resistor

Parasitic Inductance

Parasitic Capacitance

Discharge

Device under Test

Charge Resister > 10M Ω

Ground Plate

Distributed Device Body to Ground Plate Capacitance

High Voltage Source

ESD Mode

CDM：Charged-Device Mode

50Ω Semi-Rigid Coaxial Cable

Top Ground Plane

FR-4

Support Arm

Radial 1Ω Resistor

Pogo Probe

Insulating Fixture

Device under Test

Field-Charging Electrode

300MΩ Charging Resistor

High Voltage Power Supply

Discharged Current

Comparison HBM, MM and CDM pulse

I [A]

20
15
10
5
0
-5
-10

1kV CDM
2kV HBM
200V MM

0 10 20 30 40 50

time [ns]

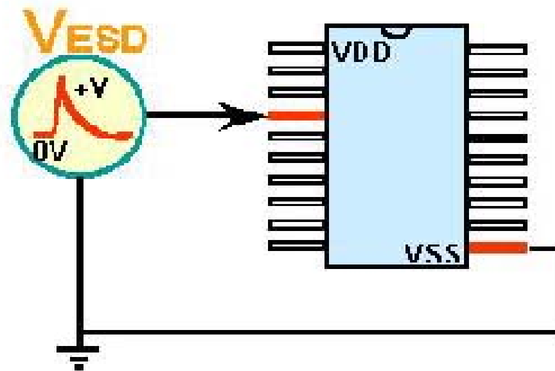
Test Level

	人體放電模式 (Human-Body Model)	機器放電模式 (Machine Model)	元件充電模式 (Charged-Device Model)
OK	2KV	200V	1KV
Save	4KV	400V	1.5KV
Super	10KV	1000V	2KV

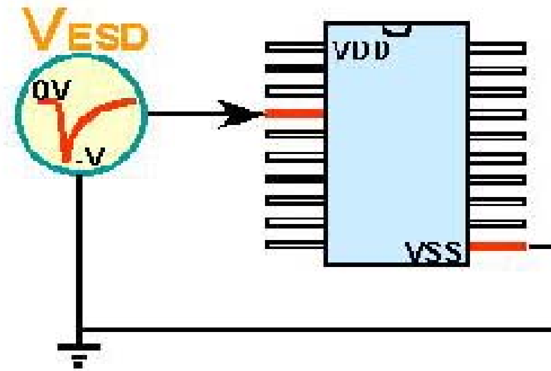
Test Method

The kinds of pin combination – I/O

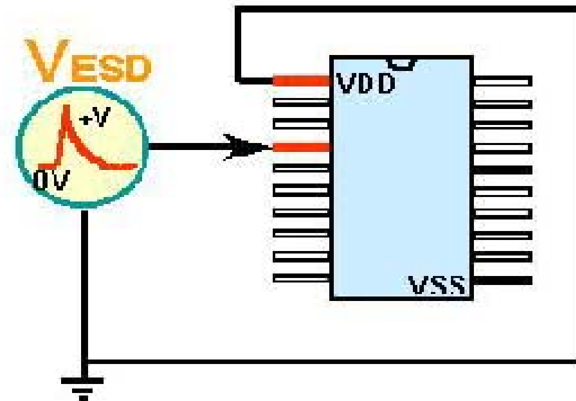
(1) PS-mode



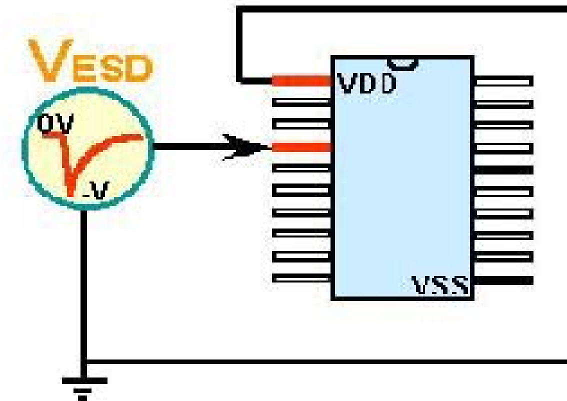
(2) NS-mode



(3) PD-mode



(4) ND-mode



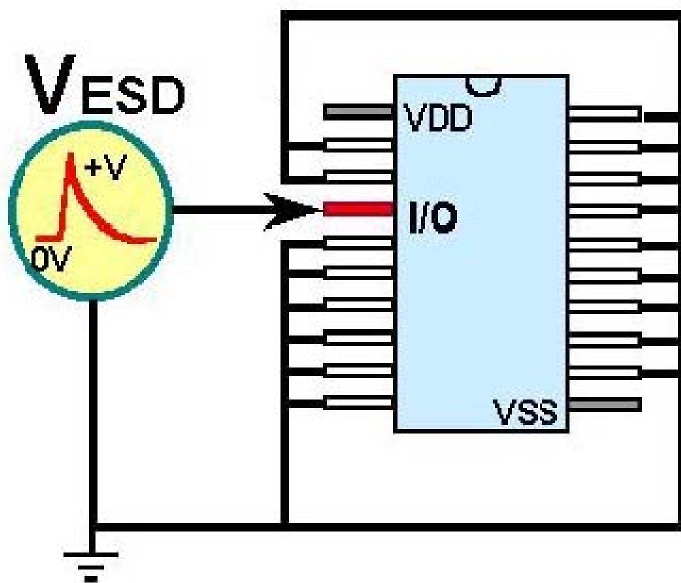
Test Method

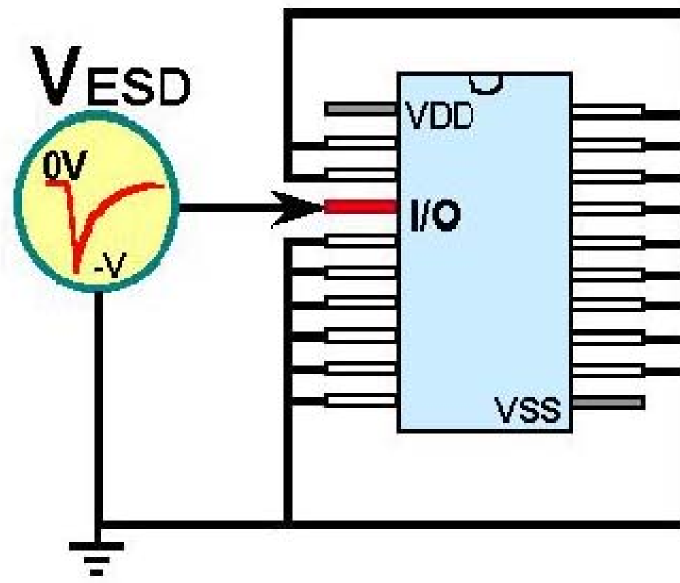
The kinds of pin combination – I/O

- **Pin-to-Pin ESD Stress :**

(1) Positive-mode

(2) Negative-mode



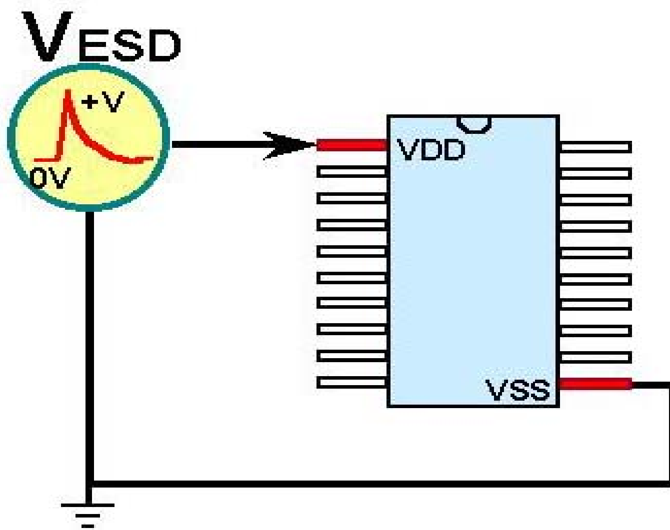


Test Method

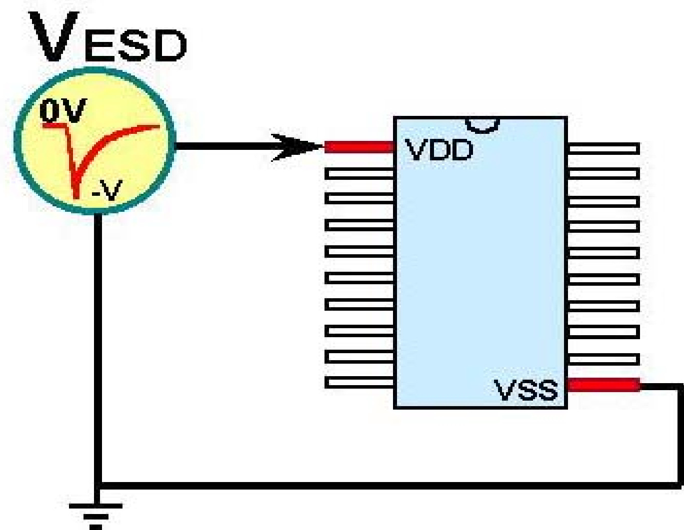
The kinds of pin combination

● VDD-to-VSS ESD Stress :

(1) Positive-mode



(2) Negative-mode

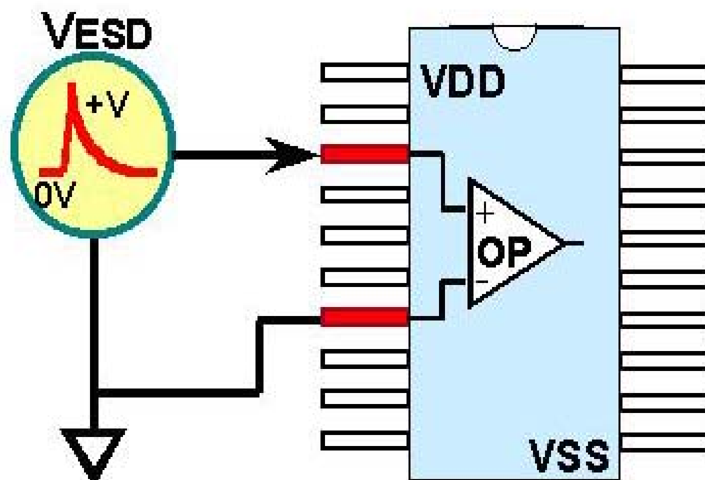


Test Method

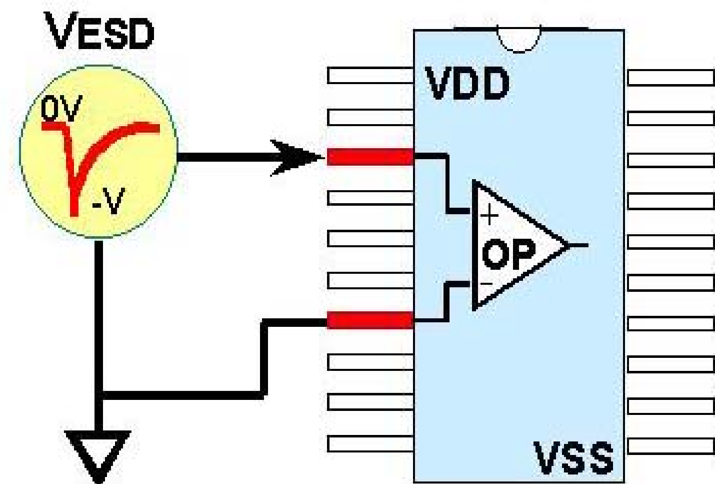
The kinds of pin combination

- ESD stress between the analog input pins of an Operational Amplifier :

(1) Positive-mode



(2) Negative-mode



Test Method
Testing Process

- Stress number = 3 Zaps. (5 Zaps, the worst case) . 1 zap/per sec.
- Stress step
  - ΔV_{ESD} = 50V(100V) for V_{ZAP} <=1000V
  - ΔV_{ESD} = 100V(250V, 500V) for V_{ZAP} > 1000V
- Starting V_{ZAP} = 70% of averaged ESD failure threshold (V_{ESD})

Test Method
Failure Decision

- 絕對漏電流
  - 當IC被ESD測試後，其Input/Output腳的漏電電流超過1μA(或10μA)。漏電電流會隨所加的偏壓大小增加而增加，在測漏電電流時所加的偏壓有人用5.5V(VDDX1.1)，也有人用7V(VDDX1.4)
- 相對I-V漂移
  - 當IC被ESD測試後，自Input/Output腳看進IC內部的I-V特性曲線漂移量在30% (20%或40%)
- 功能觀測法
  - 先把功能正常且符合規格之IC的每一支腳依測試組合打上某一電壓準位的ESD測試電壓，再拿去測試其功能是否仍符合原來的規格

Latch-up

- Overview
- Physical Origin of Latch-up
- Latch-up Triggering
- Latch-up Prevention
- Latch-up Testing

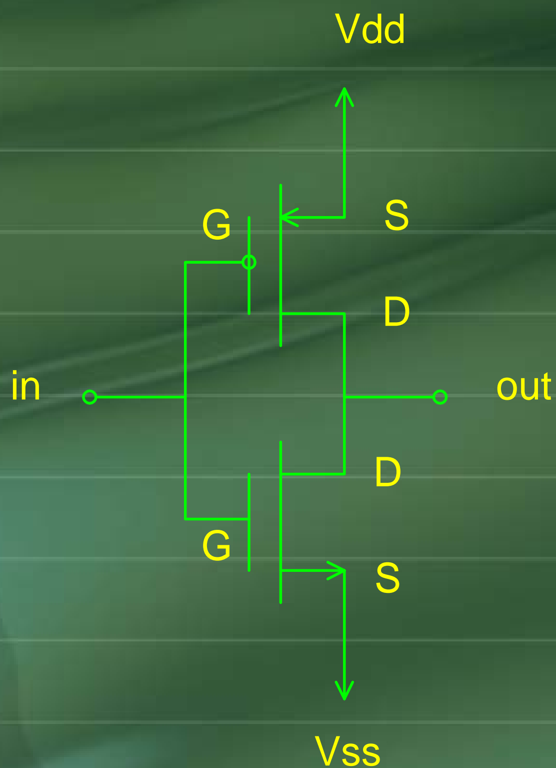
Latch-up
Overview

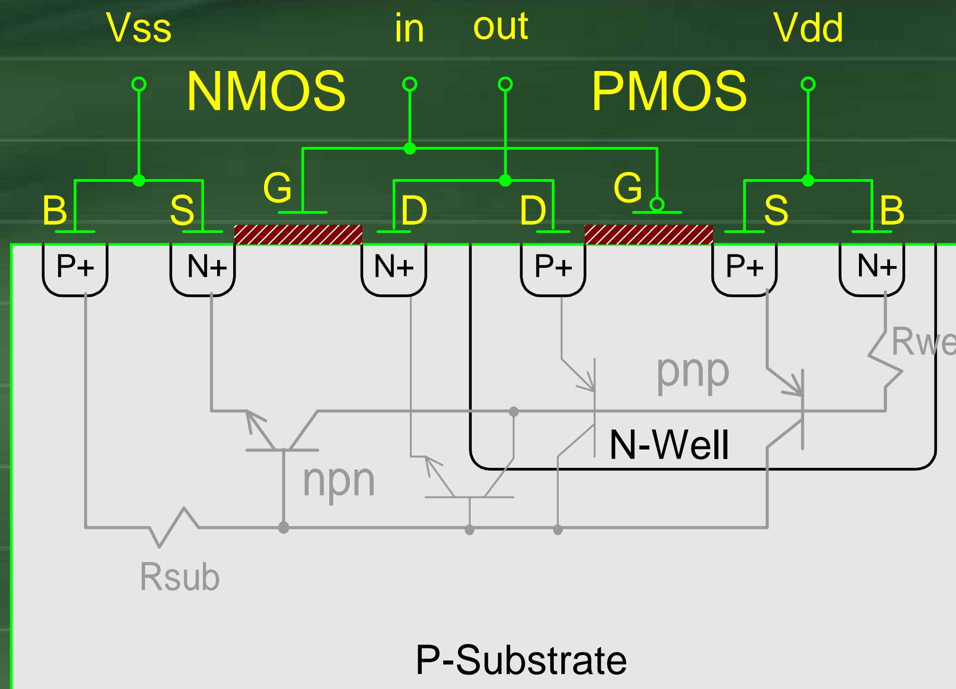
- Happened just in CMOS technology
  - N^+ + P_well or P^+ + N_well
- Via parasitic circuit effect
  - npn + pnp BJT
- Resulting in shorting of the V_{DD} and V_{SS}
- Triggered by transient voltage or current, but stop by current
- Positive feedback
- Chip will self-destruction or system failure

Latch-up

Physical Origin of Latch-up

- CMOS Inverter



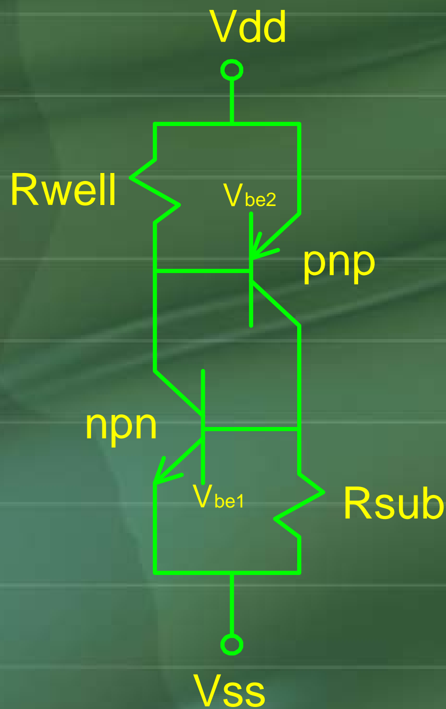


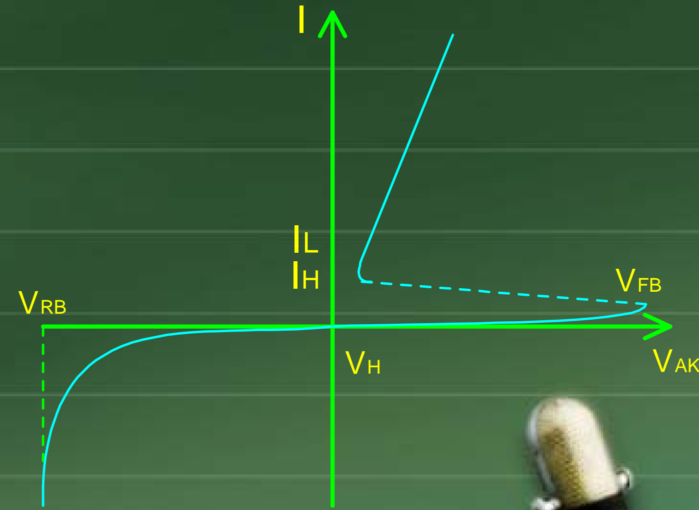
Latch-up

Physical Origin of Latch-up

- Parasitic Circuit

SCR





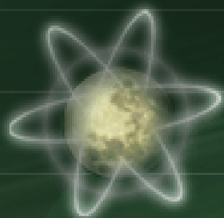
V_{FB}=Forward Breakdown voltage
V_{RB}=Reverse Breakdown voltage
V_H=Holding voltage
I_L=Latching current
I_H=Holding current

Latch-up

Latch-up Triggering

- Latch-up Triggering
  - lateral triggering
    - a sufficient current is injected into the emitter of the lateral npn-transistor
  - vertical triggering
    - a sufficient current is injected into the emitter of the vertical pnp-transistor, and the current is multiplied by the common-base-current gain

Current has to be injected either npn or pnp-emitter to initiate latchup, these conditions may occur at the I/O circuits employed on a CMOS chip



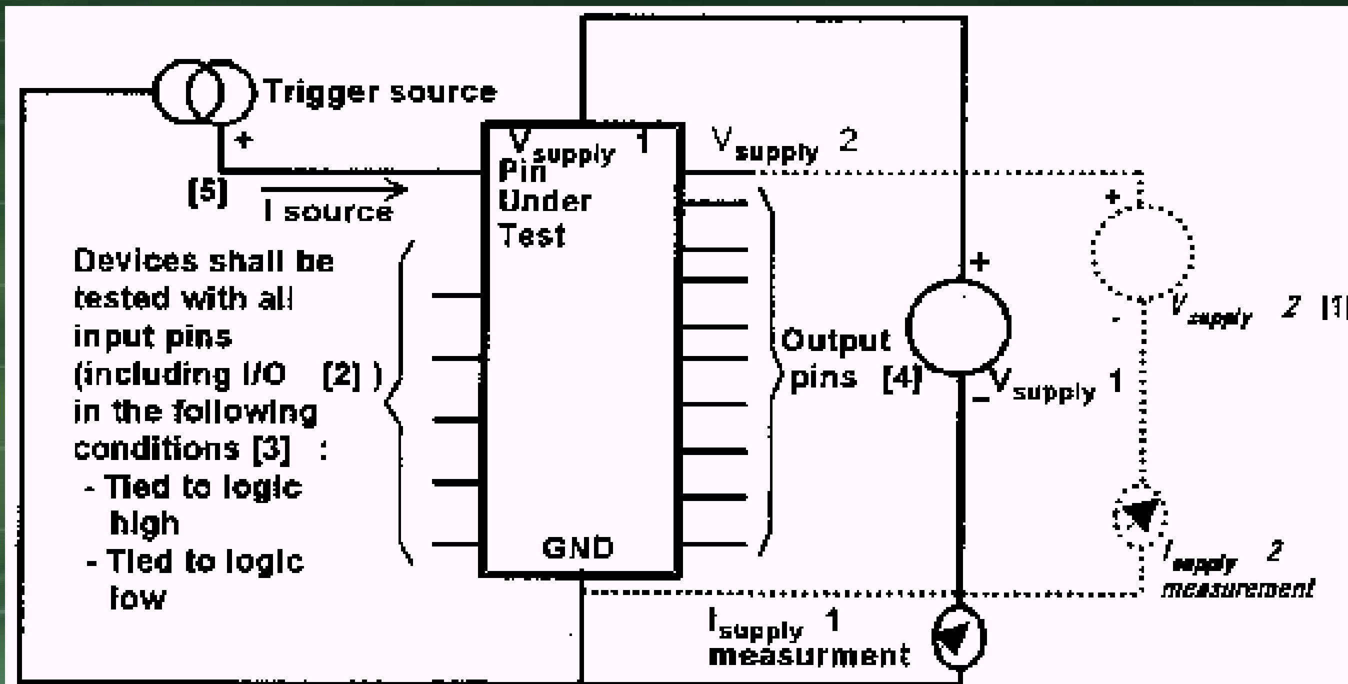
Latch-up

Latch-up Prevention

- Latch-up Prevention
  - Reducing the resistor values
  - Reducing the gain of the parasitic transistor
- Two basic way
  - Latch-up resistant CMOS process
  - Layout techniques

Latch-up

Latch-up Testing – I trigger test



1. DUT biasing shall include additional $V_{supplies}$ as required.
2. DUT shall be preconditioned so that all I/O pins are placed in a valid state per 4.1. I/O pins in the output state shall be open circuit.
3. Logic high and logic low shall be per the device specification. When logic levels are used in respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specifications, unless these conditions violate device setup condition requirements.
4. Output pins shall be open circuit except when latch-up tested.
5. The trigger test condition is defined in figure 2 and table 1.

NOTE: Dynamic devices may have timing signals applied per 4.2.3.

Latch-up

Latch-up Testing – positive I waveform

Max. V_{supply}

GND

V_{supply} PIN

+(I nom + 100 mA) or +1.5X I nom, whichever is greater

TOS

TOS

90%

Max. Logic High **

TOS

10%

t_r t_f t_r

GND

PIN UNDER TEST

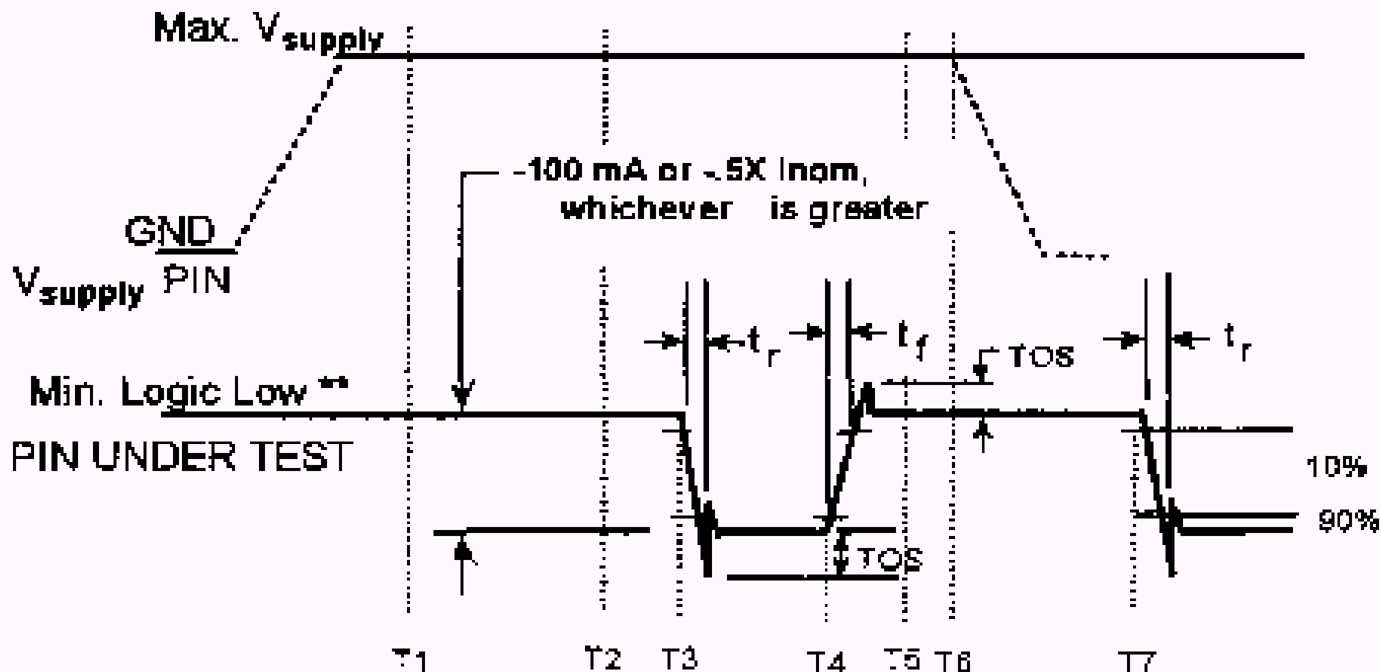
T1 T2 T3 T4 T5 T6 T7

I trigger

Time	Operation
T1 → T2	Measure nominal I_{supply} (Inom)
T4 → T7	Cool down time (Tcool)
T4 → T5	Wait time prior to I_{supply} measurement. *
T5	Measure I_{supply}
T6	If any $I_{supply} \geq$ the failure criteria defined in 1.3, latch-up has occurred and power must be removed from DUT.

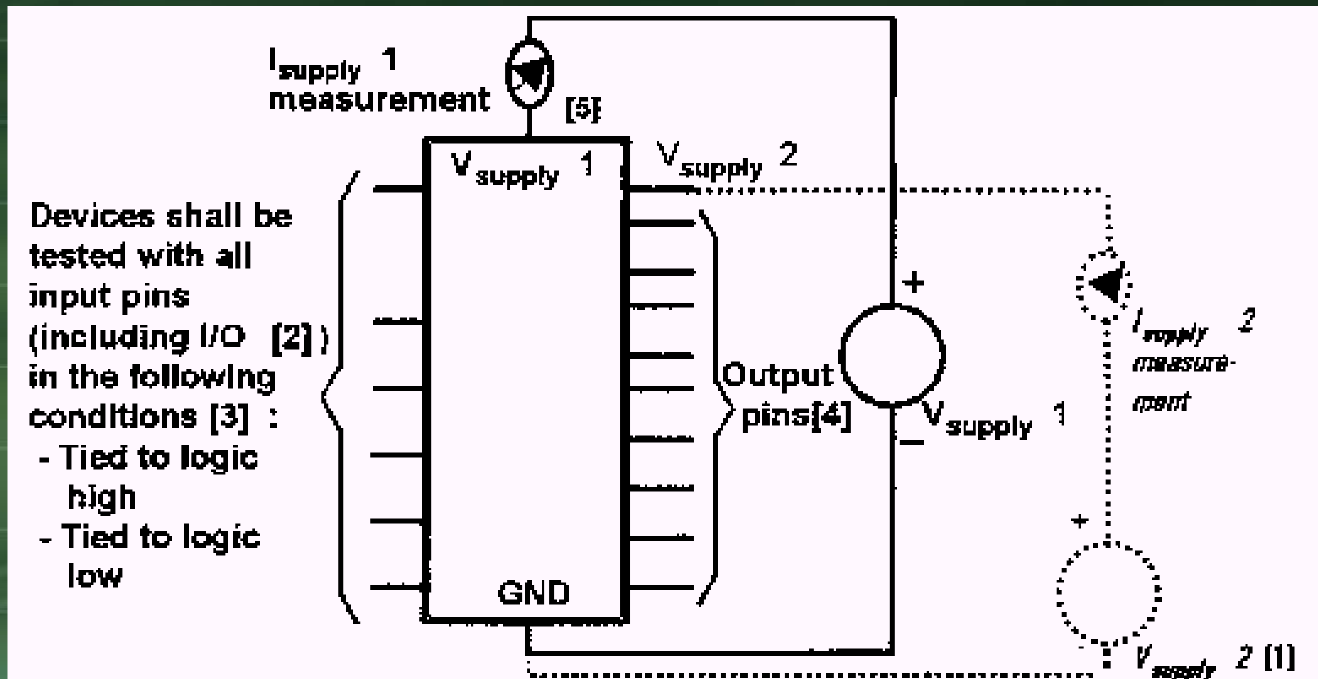
Latch-up

Latch-up Testing -- negative I waveform



Latch-up

Latch-up Testing -- V trigger test

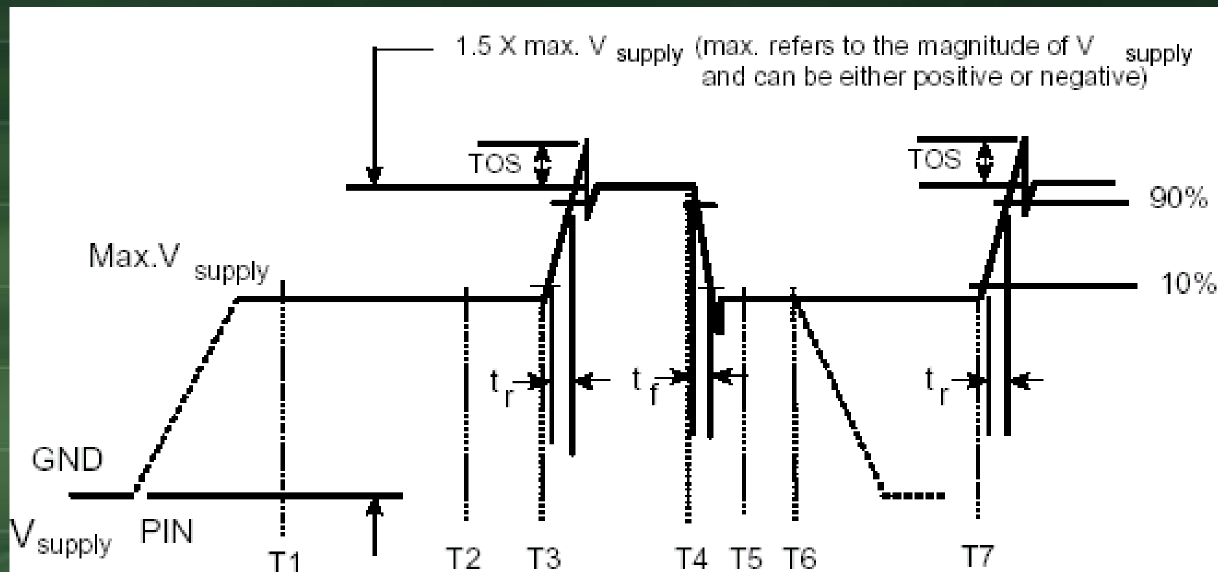


1. DUT biasing shall include additional $V_{supplies}$ as required.
2. DUT shall be preconditioned so that all I/O pins are placed in a valid state per 4.1. I/O pins in the output state shall be open circuit.
3. Logic high and logic low shall be per the device specification. When logic levels are used in respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specification, unless these conditions violate the device setup condition requirements.
4. Output pins shall be open circuit except when latch-up tested.
5. The trigger test condition is defined in figure 4 and table 1.

NOTE: Dynamic devices may have timing signals applied per 4.2.3.

Latch-up

Latch-up Testing -- V_{Supply} waveform



Time	Operation
T1 → T2	Measure nominal I_{supply} (Inom)
T4 → T7	Cool down time (Tcool)
T4 → T5	Wait time prior to I_{supply} measurement. *
T5	Measure I_{supply}
T6	If any I_{supply} ≥ the failure criteria defined in 1.3, latch-up has occurred and power must be removed from

* Note: The wait time shall be sufficient to allow for power supply ramp down and stabilization of I_{supply}

Latch-up

Latch-up Testing – timing spec.

Symbol	Time Interval	Parameter	Limits	
			Min.	Max.
t_r		Trigger rise time	5us	5ms
t_f		Trigger fall time	5us	5ms
T_{width}	T3 → T4	Trigger duration	2tr	1s
T_{OS}		Trigger over-shoot	±5% of pulse voltage	
T_{cool}	T4 → T7	Cool down time	≥ T_{width}	
$T_{measure}$	T4 → T5	Waiting time before measuring I_{supply}	3ms	5s